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Zero Voltage Switching Criteria of Triple Active Bridge Converter

Pavel Purgat‡, Soumya Bandyopadhyay‡, Zian Qin‡, and Pavol Bauer‡
‡ DC Systems Energy Conversion & Storage, Faculty of Electrical Engineering, Mathematics, and Computer Science
Delft University of Technology

***Abstract*—Triple active bridge (TAB) as an isolated multi-port converter is a promising integrated energy system for smart grids or electric vehicles. This paper aims to derive and analyse zero voltage switching (ZVS) regions of TAB, in which both switching losses are reduced, and EMI issues are mitigated. In the proposed closed-form solution of ZVS criteria, parameters such as the parasitic capacitance of the switches, the leakage inductance of the transformer, the switching frequency, the port voltage, the phase-shift inside and between the full-bridges are all taken into account. The analysis shows how the five degrees of freedom can be used to maintain ZVS operation in various operating points. The analysis and derived closed-form ZVS criteria are experimentally verified using a laboratory prototype. The derived analytical ZVS criteria are a powerful tool to study and optimise the operation of TAB converters.**

***Index Terms*— bidirectional power flow, dc-dc converters,, triple active bridge, smart grids, zero voltage switching**

I. Introduction

HIGH penetration of renewable energy sources and storage in recent years brought increase interest in multi-port converters (MPC) as a potential solution for versatile energy management systems [1]. The MPCs can integrate multiple sources, storages, and loads with varied voltage and current ratings into a single power stage allowing multi-directional power flow between its ports. Therefore, potential applications for the MPCs range from electric vehicles [2], more-electric aircrafts [3], [4] to (dc) smart grids [5], [6].

Specific applications such as EV charging require galvanic isolation between the different ports due to safety [7]. Hence, a multi-winding high-frequency (HF) transformer is used to realize this galvanic isolation required for the MPCs. One of the promising topologies in the multi-winding transformer-coupled MPC family is the triple-active bridge (TAB) converter. The TAB converter is an MPC with three full bridges connected via a high frequency (HF) multi-winding transformer [7]–[9]. Derived from the dual-active bridge (DAB) converter family [10], the TAB converter integrates and exchanges the energy from/to all ports and provides full isolation among all ports and can match the different port voltage levels.

The basic TAB modulation uses 50% duty cycles on all three full bridges and uses the phase-shifts across the three leakage inductors to transfer power between the ports [11]. However, operating with only two independent degrees of freedom leads to loss of soft-switching and high circulating currents in the HF link [11], [12]. Similarly, in DAB converters operating with a single phase-shift leads to loss of soft-switching and higher current stress. Different dual phase-shifts modulations [13]–[15] and triple phase-shift modulations [16]–[18] were proposed for DAB to increase the operating efficiency. The soft-switching areas of DAB converters operated with all three degrees of freedom were identified using various approaches [19]–[25]. Firstly, many approaches use steady-state time-domain analysis or small-signal state-space modeling techniques [25], [26]. Using the time domain analysis DAB operation was characterized into twelve operating modes in [27] and later simplified into five operating modes using graphical method in [28]. Furthermore, computationally intensive numerical approaches that incorporate the effect of parasitic capacitances were used to derive ZVS boundaries [23]. Lastly, the impact of parasitic capacitance was taken into account using energy balance equations [24]. However, due to the higher number of degrees of freedom and superpositions of port voltages applied to a transformer, the TAB converters have several tens of operating modes. The complexity makes the use of graphical methods such as [28] or computational intensive methods such as [23] less insightful.

For TAB converters, the work rigorously deriving and analyzing the soft-switching boundaries is virtually nonexistent. A derivation of soft-switching boundaries for a three-port converter without considering the effect of parasitic capacitors and only considering the basic phase-shifts are described in [29]. Moreover, due to not considering the superposition of voltages on the transformer, the listed conditions in [29] are not complete. Derivation of ZVS for a three-port topology made of half-bridges is in [12]. Again, the effect of parasitic capacitances is not considered. The soft-switching conditions under all five independent degrees of freedom and taking into account the effect of parasitic capacitances were not yet derived and analyzed.

The ZVS condition analysis includes two steps: the first step is to express the transformer currents as a function of the port voltages, phase shift angles, switching frequency, and leakage inductance. The second step is to identify all the commutation modes of the converters. In each commutation mode, calculate the minimum current that is sufficient to discharge the switch's output capacitor that is going to turn on. In the available

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Corresponding Author: Zian Qin (z.qin-2@tudelft.nl) T +421 907395264, F +31 (0)152782969 Mekelweg 4, 2628CD Delft, The Netherlands

literature, two approaches for the first step can be found: piece-wise expression or harmonic form expression of transformer currents. A piece-wise expression is easy to understand [14]; however, implementing it in a digital controller is somewhat complicated, since the expression changes in each switching pattern. The implementation becomes even more involved with increasing number of switching patterns when the modulation changes from a single-phase shift to a dual-phase shift or further to a triple-phase shift. Thank to [22], harmonic form expression is a kind of unified interpretation of the transformer current no matter which switching pattern it is in or which modulation is used. It, therefore, makes expression more concise and the implementation in the digital controller much more straightforward.

Yet, from the dual active bridge to the triple active bridge, there is a gap. Since one more port is added, there are three more parameters as the transformer's input current expressions, including the port voltage, duty cycle, and phase shift angle. Moreover, adding the third port is not an extension of a dual active bridge in terms of the transformer currents or ZVS conditions. Since the third port is highly coupled with the initial two ports, the transformer current expressions and ZVS conditions of even the initial two ports are entirely changed. Thus, the ZVS condition analysis in triple active bridge converters can hardly be found in the literature. As a result, this paper demonstrates a concise and straightforward approach to analyze the ZVS criteria of TAB: firstly, all the operation scenarios are categorized into four commutation modes; then, in each mode, Thevenin Equivalence is applied to effectively address the minimum discharging current for each port meanwhile taking into account the coupling between the port voltages and leakage inductances; eventually, by the harmonic form expression of the transformer currents, the ZVS conditions can be calculated. Experimental results are obtained under various voltage ratios and phase shift angles to validate the analysis.

The rest of this paper is organized as follows. Section II recapitulates the operating principles and modeling of the TAB converter. In section III, the soft-switching boundaries of the TAB converter are derived, analyzed, and discussed. Section IV provides experimental validation of the ZVS boundaries derived in Sections III. Section V summarises the paper and provides an outlook on the application of the presented work.

II. Operation & Modelling

A. Operating Principles

Fig. 1 shows the schematic of the TAB converter. Conceptually, the converter can be viewed as a network of inductors driven by voltage sources with controlled phase-shifts. The inductors can be inserted as separate components, or the transformer leakage inductances can be used. The simplified schematic of the converter is shown in Fig. 2. Figure 2 also shows the transformation of the transformer and the inductor network from a Y-model into Δ-model.

Throughout this paper, Δ-model is used to analyse the operation of TAB. As was done in [7], the link inductances in Δ-model can be computed from the individual leakage inductances of the transformer windings in Y-model as

$$L_{\sigma,12} = L_{\sigma,1} + L_{\sigma,2} + \frac{L_{\sigma,1}L_{\sigma,2}}{L_{\sigma,3}}, \tag{1}$$

$$L_{\sigma,13} = L_{\sigma,1} + L_{\sigma,3} + \frac{L_{\sigma,1}L_{\sigma,3}}{L_{\sigma,2}}, \tag{2}$$

$$L_{\sigma,23} = L_{\sigma,3} + L_{\sigma,2} + \frac{L_{\sigma,3}L_{\sigma,2}}{L_{\sigma,1}}, \tag{3}$$

where $L_{\sigma,2} = N^2 L'_{\sigma,2}$, $L_{\sigma,3} = N^2 L'_{\sigma,3}$ and N is the transformer ratio. Similarly, the transformer currents of the TAB converter after transformation are

$$i_{\sigma,1} = i_{\sigma,12} + i_{\sigma,13}, \tag{4}$$

$$i_{\sigma,2} = -i_{\sigma,12} + i_{\sigma,23}, \tag{5}$$

$$i_{\sigma,3} = -i_{\sigma,13} - i_{\sigma,23}, \tag{6}$$

where $i_{\sigma,1}$ is the primary side transformer current and $i_{\sigma,2} = \frac{i'_{\sigma,2}}{N}$, $i_{\sigma,3} = \frac{i'_{\sigma,3}}{N}$ are the secondary side transformer currents. The transformer ratio is accounted in voltages as $v_2 = Nv'_2$ and $v_3 = Nv'_3$.

The power flow in TAB converter can be controlled by six variables including: (a) two phase-shift angles between two port ac voltages (φ_{xy}),(b) three duty-cycles of each port α_x, and (c) switching frequency (f_s). The switching frequency variation is not used in this paper as it can lead to operation in extremely high frequency at very light loads. TAB converter operated with phase-shift between the full-bridges or ports φ_{xy} and phase-shift between the half-bridges or phase legs α_x inside each full-bridge will be analyzed in the paper.

B. Fourier Series Model

The port ac voltages v_1, v_2 and v_3 can be described using Fourier series [22]. The infinite sums describing the port voltages are

$$v_1(t) = \sum_{\substack{1\le n<\infty \\ n \text{ odd}}} \left[V_1 d_{1,r} \frac{\sin(nt\omega_s)}{n} \right], \tag{7}$$

$$v_2(t) = \sum_{\substack{1\le n<\infty \\ n \text{ odd}}} \left[V_2 d_{2,i} \frac{\cos(nt\omega_s)}{n} + V_2 d_{2,r} \frac{\sin(nt\omega_s)}{n} \right], \tag{8}$$

$$v_3(t) = \sum_{\substack{1\le n<\infty \\ n \text{ odd}}} \left[V_3 d_{3,i} \frac{\cos(nt\omega_s)}{n} + V_3 d_{3,r} \frac{\sin(nt\omega_s)}{n} \right], \tag{9}$$

where $\omega_s = 2\pi f_s$ and

$$d_{1,r} = \frac{4}{\pi} \cos\left(\frac{n\alpha_1}{2}\right), \tag{10}$$

$$d_{2,r} = \frac{4}{\pi} \cos\left(\frac{n\alpha_2}{2}\right) \cos(n\varphi_{12}), \tag{11}$$

$$d_{2,i} = \frac{4}{\pi} \cos\left(\frac{n\alpha_2}{2}\right) \sin(n\varphi_{12}), \tag{12}$$

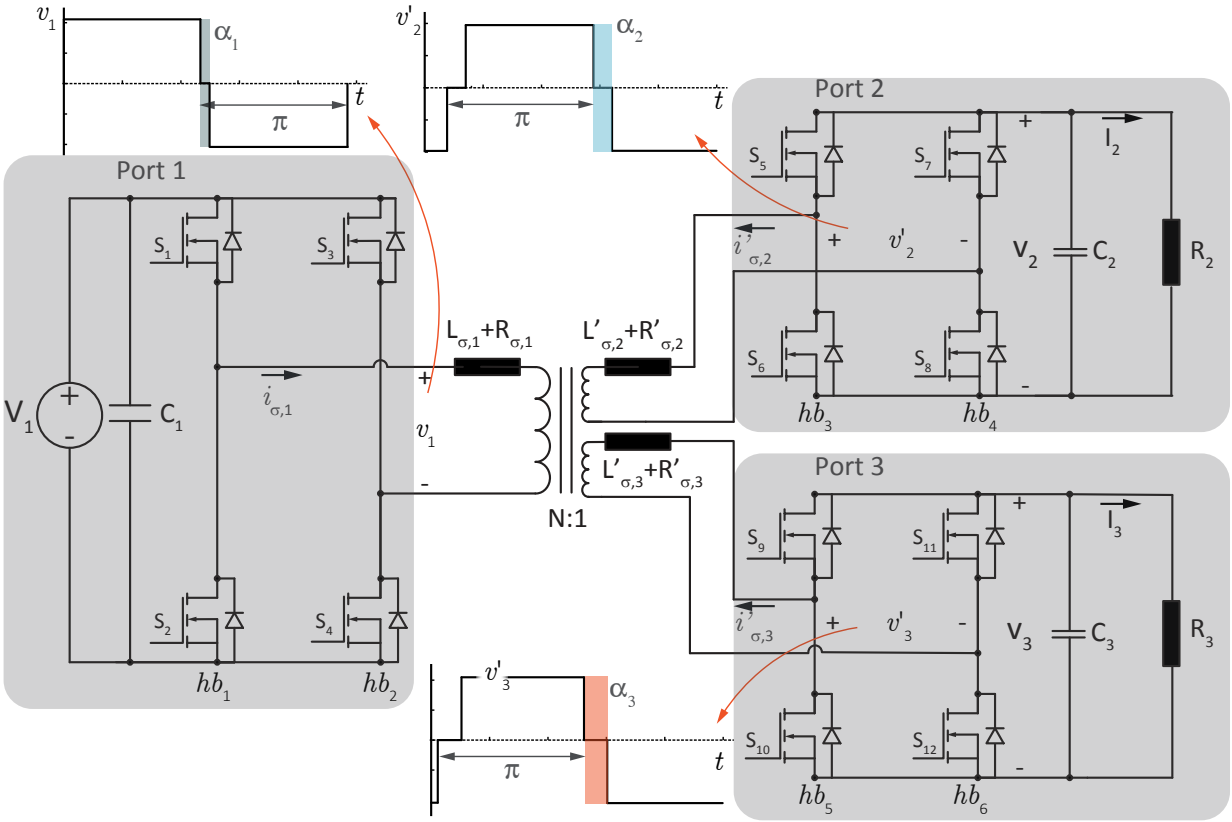


Fig. 1: Triple Active Bridge (TAB) converter schematic

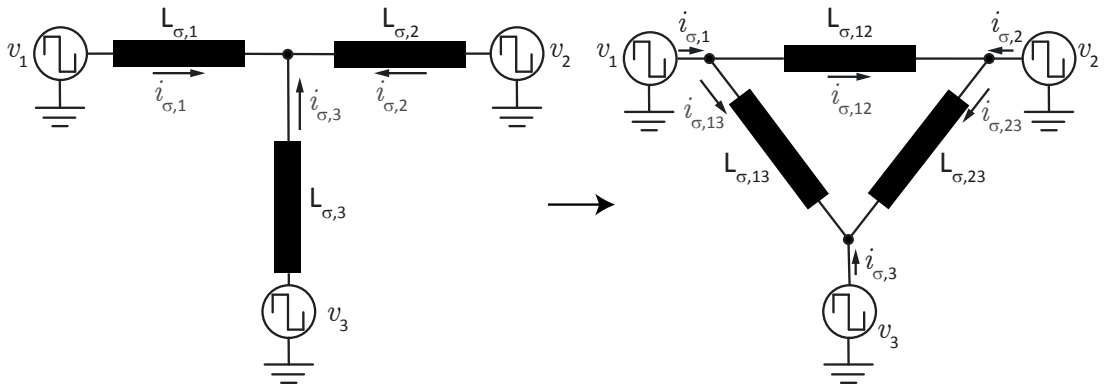


Fig. 2: Delta transformation.

$$d_{3,r} = \frac{4}{\pi}\cos\left(\frac{n\alpha_3}{2}\right)\cos\left(n\varphi_{13}\right), \tag{13}$$

$$d_{3,i} = \frac{4}{\pi}\cos\left(\frac{n\alpha_3}{2}\right)\sin\left(n\varphi_{13}\right). \tag{14}$$

The definition of φ_{12}, φ_{13} and α_1, α_2, α_3 is graphically demonstrated in Fig. 3.

The inductor currents in the circuit described in delta convention can be calculated as

$$i_{\sigma,xy}(t) - i_{\sigma,xy}(0) = \frac{1}{L_{\sigma,xy}}\int_0^t \left[v_x(\tau) - v_y(\tau)\right]\mathrm{d}\tau, \tag{15}$$

considering the switching symmetry across the switching cycle it is clear that current at $t = 0$ is the same as the current at $t = \frac{\pi}{2\omega_s}$, i.e. $i_{\sigma,xy}(\frac{\pi}{2\omega_s}) = i_{\sigma,xy}(0)$. The transformer current in delta circuit can be written as

$$i_{\sigma,12}(t) = \frac{-V_2}{L_{\sigma,12}\omega_s}\sum_{\substack{1\le n<\infty \\ n \text{ odd}}}\left[m_{12}d_{1,r}\frac{\cos\left(nt\omega_s\right)}{n^2} - d_{2,r}\frac{\cos\left(nt\omega_s\right)}{n^2} + d_{2,i}\frac{\sin\left(nt\omega_s\right)}{n^2}\right], \tag{16}$$

TABLE I: Closed-form solution of the port ac currents

Current	Closed-form solution
$i_{\sigma,1}(\tau_j)$	$-\frac{\pi V_2}{2\omega_s L_{\sigma,12}}\left[1+m_{12}\left(\frac{\left\lvert\frac{\alpha_1}{2}+\tau_j\right\rvert+\left\lvert\frac{-\alpha_1}{2}+\tau_j\right\rvert}{\pi}-1\right)-\frac{\left(\left\lvert\frac{\alpha_2}{2}+\tau_j-\varphi_{12}\right\rvert+\left\lvert-\frac{\alpha_2}{2}+\tau_j-\varphi_{12}\right\rvert\right)}{\pi}\right]+$ $\frac{-\pi V_3}{2\omega_s L_{\sigma,13}}\left[1+m_{13}\left(\frac{\left\lvert\frac{\alpha_1}{2}+\tau_j\right\rvert+\left\lvert\frac{-\alpha_1}{2}+\tau_j\right\rvert}{\pi}-1\right)-\frac{\left(\left\lvert\frac{\alpha_3}{2}+\tau_j-\varphi_{13}\right\rvert+\left\lvert-\frac{\alpha_3}{2}+\tau_j-\varphi_{13}\right\rvert\right)}{\pi}\right]$
$i_{\sigma,2}(\tau_j)$	$\frac{\pi V_2}{2\omega_s}\left[\frac{1}{L_{\sigma,12}}\left[1+m_{12}\left(\frac{\left\lvert\frac{\alpha_1}{2}+\tau_j\right\rvert+\left\lvert\frac{-\alpha_1}{2}+\tau_j\right\rvert}{\pi}-1\right)-\frac{\left(\left\lvert\frac{\alpha_2}{2}+\tau_j-\varphi_{12}\right\rvert+\left\lvert-\frac{\alpha_2}{2}+\tau_j-\varphi_{12}\right\rvert\right)}{\pi}\right]+\right.$ $\left.\frac{-1}{L_{\sigma,23}}\left[\frac{1}{m_{23}}\left(1-\frac{\left\lvert\frac{\alpha_3}{2}+\tau_j-\varphi_{13}\right\rvert+\left\lvert\frac{\alpha_3}{2}-\tau_j+\varphi_{13}\right\rvert}{\pi}\right)+\frac{\left\lvert\frac{\alpha_2}{2}+\tau_j-\varphi_{12}\right\rvert+\left\lvert\frac{\alpha_3}{2}-\tau_j+\varphi_{12}\right\rvert}{\pi}-1\right]\right]$
$i_{\sigma,3}(\tau_j)$	$\frac{\pi V_3}{2\omega_s}\left[\frac{1}{L_{\sigma,13}}\left[1+m_{13}\left(\frac{\left\lvert\frac{\alpha_1}{2}+\tau_j\right\rvert+\left\lvert\frac{-\alpha_1}{2}+\tau_j\right\rvert}{\pi}-1\right)-\frac{\left(\left\lvert\frac{\alpha_3}{2}+\tau_j-\varphi_{13}\right\rvert+\left\lvert-\frac{\alpha_3}{2}+\tau_j-\varphi_{13}\right\rvert\right)}{\pi}\right]+\right.$ $\left.\frac{1}{L_{\sigma,23}}\left[m_{23}\left(\frac{\left\lvert\frac{\alpha_2}{2}+\tau_j-\varphi_{12}\right\rvert+\left\lvert\frac{\alpha_2}{2}-\tau_j+\varphi_{12}\right\rvert}{\pi}-1\right)-\frac{\left(\left\lvert\frac{\alpha_3}{2}+\tau_j-\varphi_{13}\right\rvert+\left\lvert\frac{\alpha_3}{2}-\tau_j+\varphi_{13}\right\rvert\right)}{\pi}-1\right]\right]$

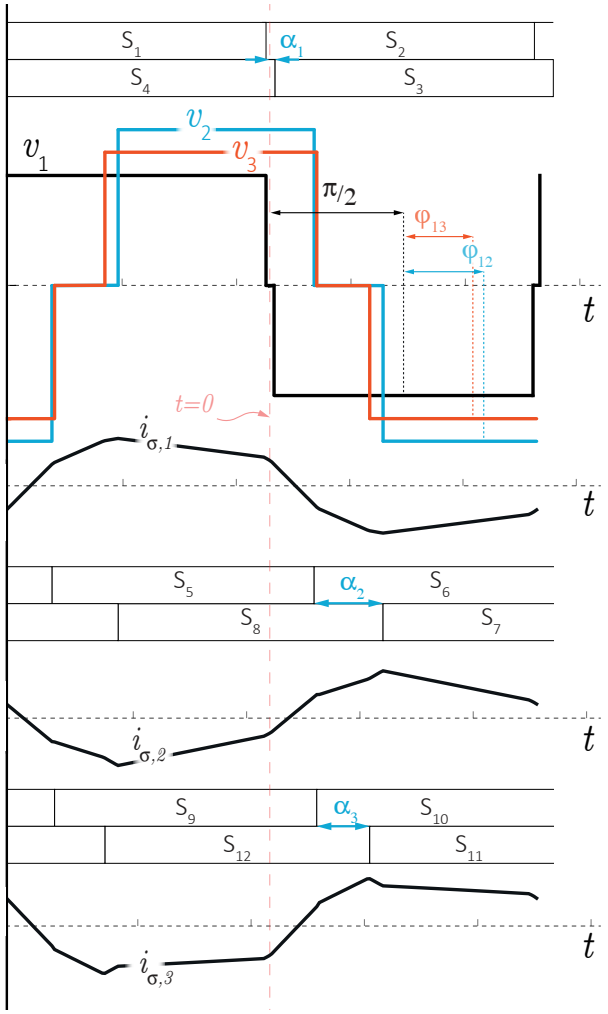


Fig. 3: Phase leg switched voltages and port currents during commutation.

$$i_{\sigma,13}(t) = \frac{-V_3}{L_{\sigma,13}\omega_s}\sum_{\substack{1\le n<\infty \\ n \text{ odd}}}\left[m_{13}d_{1,r}\frac{\cos(nt\omega_s)}{n^2} - d_{3,r}\frac{\cos(nt\omega_s)}{n^2} + d_{3,i}\frac{\sin(nt\omega_s)}{n^2}\right], \tag{17}$$

$$i_{\sigma,23}(t) = \frac{-V_3}{L_{\sigma,23}\omega_s}\sum_{\substack{1\le n<\infty \\ n \text{ odd}}}\left[m_{23}\left(d_{2,r}\frac{\cos(nt\omega_s)}{n^2} - d_{2,i}\frac{\sin(nt\omega_s)}{n^2}\right) - d_{3,r}\frac{\cos(nt\omega_s)}{n^2} + d_{3,i}\frac{\sin(nt\omega_s)}{n^2}\right], \tag{18}$$

where $m_{12} = \frac{V_1}{V_2}$, $m_{13} = \frac{V_1}{V_3}$ and $m_{23} = \frac{V_2}{V_3}$.

C. Closed Form Solution

By substituting the harmonic form expression of the delta circuit currents in (16)-(18) and duty cycle in (10)-(14), into the port currents in (4)-(6), the closed-form solution of the port current $i_{\sigma,1}(\tau_j)$, $i_{\sigma,2}(\tau_j)$ and $i_{\sigma,3}(\tau_j)$ at the events of switching transitions τ_j can be obtained, and they are summarized in Table I. The times of switching event τ_j are defined in Table IV. Note that in the derivation procedure of the closed form solution of the port currents from harmonic form expression, following properties of infinite series of odd components are used [22],

$$\sum_{\substack{1\le n<\infty \\ n \text{ odd}}}\frac{1}{n^2} = \frac{\pi^2}{8}, \tag{19}$$

$$\sum_{\substack{1\le n<\infty \\ n \text{ odd}}}\frac{\cos(n\beta)}{n^2} = \frac{\pi(\pi - |2\beta|)}{8}, \tag{20}$$

where β is any angle in radians.

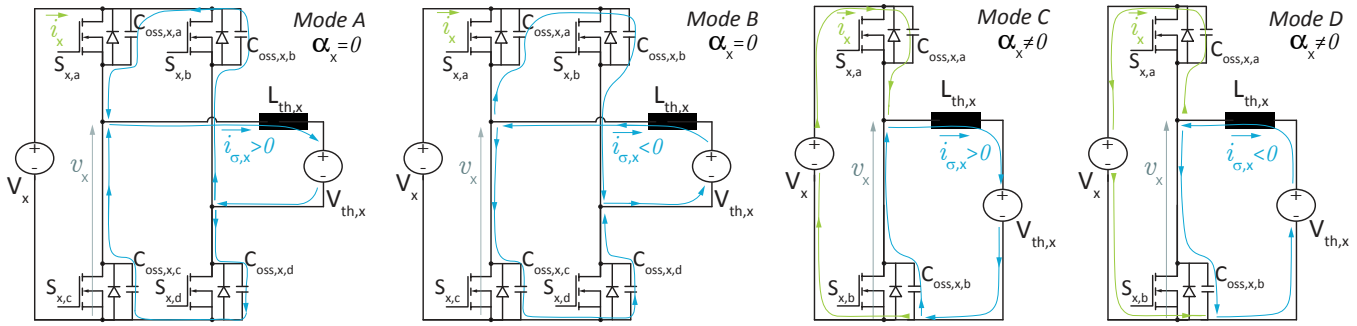


Fig. 4: Port schematics during four possible commutation modes.

TABLE II: ZVS Conditions of TAB Converter

Mode	Switches turned-on	Conditions
A	S_c and S_b	if $V_{\text{th},x} > 0$ the ZVS condition is $\lvert i_{\sigma,x}(\tau_j)\rvert \geq 2V_x\sqrt{\frac{C_{\text{oss},x}}{L_{\text{th},x}}\frac{V_{\text{th},x}}{V_x}}$
		if $V_{\text{th},x} < 0$, the ZVS is assured
B	S_a and S_d	if $V_{\text{th},x} < 0$ the ZVS condition is $\lvert i_{\sigma,x}(\tau_j)\rvert \geq 2V_x\sqrt{-\frac{C_{\text{oss},x}}{L_{\text{th},x}}\frac{V_{\text{th},x}}{V_x}}$
		if $V_{\text{th},x} > 0$, the ZVS is assured
C	S_b	if $V_{\text{th},x} > \frac{V_x}{2}$, the ZVS condition is $\lvert i_{\sigma,x}(\tau_j)\rvert \geq 2V_x\sqrt{\frac{C_{\text{oss},x}}{L_{\text{th},x}}\frac{V_{\text{th},x}}{V_x} - \frac{C_{\text{oss},x}}{2L_{\text{th},x}}}$
		if $V_{\text{th},x} < \frac{V_x}{2}$, the ZVS is assured
D	S_a	if $V_{\text{th},x} < \frac{V_x}{2}$, the ZVS condition is $\lvert i_{\sigma,x}(\tau_j)\rvert \geq 2V_x\sqrt{-\frac{C_{\text{oss},x}}{L_{\text{th},x}}\frac{V_{\text{th},x}}{V_x} + \frac{C_{\text{oss},x}}{2L_{\text{th},x}}}$
		if $V_{\text{th},x} > \frac{V_x}{2}$, the ZVS is assured

III. Zero Voltage Switching

The full-bridge ac voltages and the corresponding currents are shown in Fig. 3. In an ideal case, the energy stored in the MOSFETs parasitic capacitors is ignored, and the magnetizing inductance of the transformer is considered infinite. In this ideal case, the ZVS operation of the converter switches is only dependent on the direction of the output bridge current during the state transition. ZVS occurs when the output current of a bridge is flowing through the active switch of the corresponding half-bridge as the half-bridges opposing transistor becomes active; in such a case, the current will naturally commute to the opposing switch anti-parallel diode after the active switched is turned off.

MOSFET's parasitic capacitance adds a soft-switching condition, in the form of minimal current in the leakage inductance required to complete the ZVS commutation. To derive the ZVS conditions for the TAB converter, it is assumed that the converter operates in steady-state, i.e., only one phase leg commutates at each switching event.

TAB can be operated with five phase-shifts. Two phase-shifts between ports φ_{12}, φ_{13}, and three phase-shifts that are defined between phase legs of each port α_1, α_2 and α_3. The phase-shifts φ_{12}, φ_{13} as marked in Fig.3 are defined as the difference between the middle points of the switching cycles. These five degrees of freedom can create tens of different operating modes, and examining each with graphical tools is impractical. Therefore to analyze ZVS of a TAB converter, a comprehensive investigation of ZVS conditions for generic full-bridge operated with phase-shifts φ_x and α_x is presented. In the generic full-bridge, four separate switching modes are identified. These four modes encompass all unique commutations, i.e., the remaining commutations are always

symmetrical counter-parts of described commutations. The four commutation modes can be divided into two groups based on the phase leg phase shift α_x, and further subdivided by the direction of the port current $i_{\sigma,x}$. In second step, values of inductor $L_{\text{th},x}$ and amplitude of voltage source $v_{\text{th},x}$ in the generic full bridge are derived. The need for the second step stems from the fact that the inductor and the voltage source in the TAB converter are not simple constants (unlike in DAB), but are superpositions of each ports state at the given time instant. Therefore, Thevenin equivalents of these voltages are derived in the second step. The third step consists of synthesizing the conditions from the first step, Thevenin equivalents impedances and voltage sources, and the respective sequences of switching instances τ_j. These three steps establish conditions for ZVS in the TAB converter.

A. Mode A: $\alpha_x = 0$, $i_{\sigma,x}(\tau_j) > 0$

In mode A all four switches are commutating, $S_{x,a}$ and $S_{x,d}$ have been turned off, while $S_{x,b}$ and $S_{x,c}$ are going to be turned on. From Fig. 4a following current equations can be written

$$i_{\sigma,x}(\tau_j) = -2C_{\text{oss},x}\frac{\mathrm{d}v_x}{\mathrm{d}t}, \tag{21}$$

$$i_x(\tau_j) = 0. \tag{22}$$

The minimum current requirement for ZVS is obtained from the energy absorbed by $V_{\text{th},x}$, which can be calculated as follows

$$E_{\text{absorbed}} = \int_{T_{\text{com}}} V_{\text{th},x} i_{\sigma,x}(\tau_j)\mathrm{d}t. \tag{23}$$

Combining (21), (22) and assuming the voltage v_x is changing from V_x to 0 in (23), following is obtained

$$E_{\text{absorbed}} = 2C_{\text{oss},x}V_{\text{th},x}V_x. \tag{24}$$

The sum of energy stored in the parasitic capacitors does not change during commutation. To find the minimum current amplitude requirement, an energy inequality can be written as

$$\frac{1}{2}L_{\text{th},x}i^2_{\sigma,x}(\tau_j) \geq 2C_{\text{oss},x}V_{\text{th},x}V_x. \tag{25}$$

The polarity of the voltage $V_{\text{th},x}$ is assumed to be positive in (25). If the voltage $V_{th,x}$ is negative, then ZVS is always achieved. The minimal current condition for Mode A, when $V_{\text{th},x} > 0$ can be written as

$$|i_{\sigma,x}(\tau_j)| \geq 2V_x\sqrt{\frac{C_{\text{oss},x}}{L_{\text{th},x}}\frac{V_{\text{th},x}}{V_x}}. \tag{26}$$

B. Mode B: $\alpha_x = 0$, $i_{\sigma,x}(\tau_j) < 0$

As shown in Fig. 4b, in mode B, all four switches are commutating, where $S_{x,b}$ and $S_{x,c}$ have been turned off while $S_{x,a}$ and $S_{x,d}$ are going to be turned on. The inductor current is flowing into the full bridge, which is in reverse compared to mode A. The current equations from Fig. 4b can be written as

$$i_{\sigma,x}(\tau_j) = -2C_{\text{oss},x}\frac{\mathrm{d}v_x}{\mathrm{d}t}, \tag{27}$$

$$i_x(\tau_j) = 0. \tag{28}$$

Similarly as in mode A, following energy inequality can be derived

$$\frac{1}{2}L_{\text{th},x}i^2_{\sigma,x}(\tau_j) \geq -2C_{\text{oss},x}V_{\text{th},x}V_x. \tag{29}$$

In (29) it is assumed that $V_{\text{th},x}$ is negative, otherwise ZVS is assured. The minimal current requirement for mode B can be written as

$$|i_{\sigma,x}(\tau_j)| \geq 2V_x\sqrt{-\frac{C_{\text{oss},x}}{L_{\text{th},x}}\frac{V_{\text{th},x}}{V_x}}. \tag{30}$$

The inequality (30) is derived for switches $S_{\text{x},a}$ and $S_{\text{x},d}$ turning on.

C. Mode C: $\alpha_x \neq 0$, $i_{\sigma,x}(\tau_j) > 0$

Mode C commutation is shown in Fig. 4c. Mode C occurs when the phase-shift α_x is non-zero. The soft-switching conditions for leading and lagging phase-leg become different. According to Fig. 4c the currents are

$$i_{\sigma,x}(\tau_j) = -2C_{\text{oss},x}\frac{\mathrm{d}v_x}{\mathrm{d}t}, \tag{31}$$

$$i_x(\tau_j) = -C_{\text{oss},x}\frac{\mathrm{d}v_x}{\mathrm{d}t}. \tag{32}$$

As was done for modes A and B, calculating the absorbed energy by source $v_{th,x}$ leads to calculation of the minimum current amplitude requirement. Energy absorbed by the sources can be calculated as

$$E_{\text{absorbed}} = \int_{T_{\text{com}}} V_{\text{th},x} i_{\sigma,x}(\tau_j)\mathrm{d}t - \int_{T_{\text{com}}} V_x i_x(\tau_j)\mathrm{d}t. \tag{33}$$

Combining to (31), (32) and assuming the voltage v_x to change from V_x to 0 in (33) following is obtained

$$E_{\text{absorbed}} = 2C_{\text{oss},x}V_{\text{th},x}V_x - C_{\text{oss},x}V_x^2. \tag{34}$$

Similarly as for modes A and B, minimum current requirement can be obtained from

$$\frac{1}{2}L_{\text{th}}i^2_{\sigma,x}(\tau_j) \geq 2C_{\text{oss},x}V_{\text{th},x}V_x - C_{\text{oss},x}V_x^2, \tag{35}$$

From (35) a ZVS condition can be obtained

$$|i_{\sigma,x}(\tau_j)| \geq 2V_x\sqrt{\frac{C_{\text{oss},x}}{L_{\text{th},x}}\frac{V_{\text{th},x}}{V_x} - \frac{C_{\text{oss},x}}{2L_{\text{th},x}}}, \tag{36}$$

where $V_{\text{th},x} > \frac{V_x}{2}$ otherwise ZVS is assured for switch S_b.

D. Mode D- $\alpha_x \neq 0$, $i_{\sigma,x}(\tau_j) < 0$

The counter part of mode C is mode D which occurs when the inductor current has opposite polarity. Circuit describing mode D is shown in Fig. 4d. The current equations can be written as

$$i_{\sigma,x}(\tau_j) = -2C_{\text{oss},x}\frac{\mathrm{d}v_x}{\mathrm{d}t}, \tag{37}$$

TABLE III: Port Characteristics for ZVS Conditions of TAB Converter

Port no.	$L_{\text{th},x}$	Half-bridge	$V_{\text{th},x}$	$i_{\sigma,x}$
1	$\frac{L_{\sigma,13}L_{\sigma,12}}{L_{\sigma,13}+L_{\sigma,12}}$	Leading	$V_2(\tau_1)\frac{L_{\sigma,13}}{L_{\sigma,13}+L_{\sigma,12}} + V_3(\tau_1)\frac{L_{\sigma,12}}{L_{\sigma,13}+L_{\sigma,12}}$	$i_{\sigma,1}$
		Lagging	$-V_2(\tau_2)\frac{L_{\sigma,13}}{L_{\sigma,13}+L_{\sigma,12}} - V_3(\tau_2)\frac{L_{\sigma,12}}{L_{\sigma,13}+L_{\sigma,12}}$	$-i_{\sigma,1}$
2	$\frac{L_{\sigma,23}L_{\sigma,12}}{L_{\sigma,23}+L_{\sigma,12}}$	Leading	$V_1(\tau_3)\frac{L_{\sigma,23}}{L_{\sigma,23}+L_{\sigma,12}} + V_3(\tau_3)\frac{L_{\sigma,12}}{L_{\sigma,23}+L_{\sigma,12}}$	$i_{\sigma,2}$
		Lagging	$-V_1(\tau_4)\frac{L_{\sigma,23}}{L_{\sigma,23}+L_{\sigma,12}} - V_3(\tau_4)\frac{L_{\sigma,12}}{L_{\sigma,23}+L_{\sigma,12}}$	$-i_{\sigma,2}$
3	$\frac{L_{\sigma,13}L_{\sigma,23}}{L_{\sigma,13}+L_{\sigma,23}}$	Leading	$V_1(\tau_5)\frac{L_{\sigma,23}}{L_{\sigma,23}+L_{\sigma,13}} + V_2(\tau_5)\frac{L_{\sigma,13}}{L_{\sigma,23}+L_{\sigma,13}}$	$i_{\sigma,3}$
		Lagging	$-V_1(\tau_6)\frac{L_{\sigma,23}}{L_{\sigma,23}+L_{\sigma,13}} - V_2(\tau_6)\frac{L_{\sigma,13}}{L_{\sigma,23}+L_{\sigma,13}}$	$-i_{\sigma,3}$

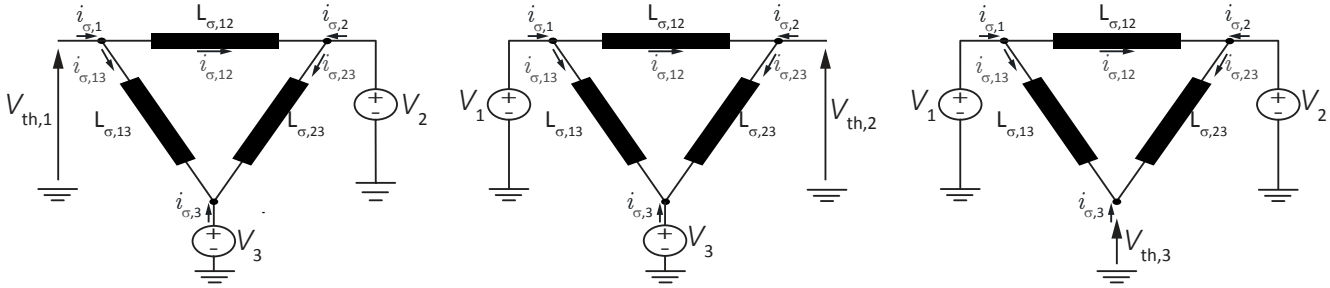


Fig. 5: Equivalent Thevenin circuits.

$$i_x(\tau_j) = -C_{\text{oss},x}\frac{\mathrm{d}v_x}{\mathrm{d}t}. \tag{38}$$

Similarly as for mode C, energy absorbed and supplied can be derived. The notable difference is the change of voltage v_x from 0 to V_x. Using the inductor and capacitances energies, minimum current amplitude requirement can be written as

$$\frac{1}{2}L_{\text{th},x}i^2_{\sigma,x}(\tau_j) \geq -2C_{\text{oss},x}V_{\text{th},x}V_x + C_{\text{oss},x}V_x^2. \tag{39}$$

From (39) the minimum amplitude current requirement can be obtained as

$$|i_{\sigma,x}(\tau_j)| \geq 2V_x\sqrt{-\frac{C_{\text{oss},x}}{L_{th,x}}\frac{V_{\text{th},x}}{V_x} + \frac{C_{\text{oss},x}}{2L_{\text{th},x}}}. \tag{40}$$

Condition (40) is derived for turn on of switch S_a when voltage $V_{\text{th},x}$ is smaller than $\frac{V_x}{2}$, otherwise ZVS is assured for S_a.

The ZVS conditions for all modes are summarized in Table II. The parameters like $V_{\text{th},x}$, $L_{\text{th},x}$ and $i_{\sigma,x}$ for the conditions are then derived as follows in Table III.

E. Thevenin Equivalent Circuits

The delta circuit from Fig. 2 is simplified into three Thevenin equivalent circuits as shown in Fig. 5. During commutation, the port voltage either remains the same or has already changed to new value, and thereby they are considered as constant voltage and expressed with uppercase letters. The values of V_x during each commucation are defined in Table IV. For illustration, the Thevenin equivalent impedance during commutation of port one can be derived from circuit in Fig. 5a. The equivalent impedance is calculated by short-circuiting V_2 and V_3 and equals

$$L_{\text{th},1} = \frac{L_{\sigma,12}L_{\sigma,13}}{L_{\sigma,12}+L_{\sigma,13}}. \tag{41}$$

The Thevenin equivalent voltage for the same circuit is a superposition of the two voltage dividers at time instant τ_1 and can be written as

$$V_{\text{th},1}(\tau_1) = V_2(\tau_1)\frac{L_{\sigma,13}}{L_{\sigma,12}+L_{\sigma,13}} + V_3(\tau_1)\frac{L_{\sigma,12}}{L_{\sigma,12}+L_{\sigma,13}}. \tag{42}$$

Thevenin equivalent impedances and voltages can be derived for other ports in similar manner, and are summarized in Table III.

TABLE IV: Switching sequences for selection of $V_{\text{th},x}$.

Port no.	Half-bridge	Voltages for Thevenin Circuit		τ_j
1	Leading	$V_2(\tau_1)=\begin{cases}V_2 & \text{if } \tau_1<\tau_3,\\ 0 & \text{if } \tau_3<\tau_1<\tau_4,\\ -V_2 & \text{if } \tau_4<\tau_1,\end{cases}$	$V_3(\tau_1)=\begin{cases}V_3 & \text{if } \tau_1<\tau_5,\\ 0 & \text{if } \tau_5<\tau_1<\tau_6,\\ -V_3 & \text{if } \tau_6<\tau_1,\end{cases}$	$\tau_1=-\frac{\alpha_1}{2}$
	Lagging	$V_2(\tau_2)=\begin{cases}V_2 & \text{if } \tau_2<\tau_3,\\ 0 & \text{if } \tau_3<\tau_2<\tau_4,\\ -V_2 & \text{if } \tau_4<\tau_2,\end{cases}$	$V_3(\tau_2)=\begin{cases}V_3 & \text{if } \tau_2<\tau_5,\\ 0 & \text{if } \tau_5<\tau_2<\tau_6,\\ -V_3 & \text{if } \tau_6<\tau_2,\end{cases}$	$\tau_2=\frac{\alpha_1}{2}$
2	Leading	$V_1(\tau_3)=\begin{cases}V_1 & \text{if } \tau_3<\tau_1,\\ 0 & \text{if } \tau_1<\tau_3<\tau_2,\\ -V_1 & \text{if } \tau_2<\tau_3,\end{cases}$	$V_3(\tau_3)=\begin{cases}V_3 & \text{if } \tau_3<\tau_5,\\ 0 & \text{if } \tau_5<\tau_3<\tau_6,\\ -V_3 & \text{if } \tau_6<\tau_3,\end{cases}$	$\tau_3=\varphi_{12}-\frac{\alpha_2}{2}$
	Lagging	$V_1(\tau_4)=\begin{cases}V_1 & \text{if } \tau_4<\tau_1,\\ 0 & \text{if } \tau_1<\tau_4<\tau_2,\\ -V_1 & \text{if } \tau_2<\tau_4,\end{cases}$	$V_3(\tau_4)=\begin{cases}V_3 & \text{if } \tau_4<\tau_5,\\ 0 & \text{if } \tau_5<\tau_4<\tau_6,\\ -V_3 & \text{if } \tau_6<\tau_4,\end{cases}$	$\tau_4=\varphi_{12}+\frac{\alpha_2}{2}$
3	Leading	$V_1(\tau_5)=\begin{cases}V_1 & \text{if } \tau_5<\tau_1,\\ 0 & \text{if } \tau_1<\tau_5<\tau_2,\\ -V_1 & \text{if } \tau_2<\tau_5,\end{cases}$	$V_2(\tau_5)=\begin{cases}V_2 & \text{if } \tau_5<\tau_3,\\ 0 & \text{if } \tau_3<\tau_5<\tau_4,\\ -V_2 & \text{if } \tau_4<\tau_5,\end{cases}$	$\tau_5=\varphi_{13}-\frac{\alpha_3}{2}$
	Lagging	$V_1(\tau_6)=\begin{cases}V_1 & \text{if } \tau_6<\tau_1,\\ 0 & \text{if } \tau_1<\tau_6<\tau_2,\\ -V_1 & \text{if } \tau_2<\tau_6,\end{cases}$	$V_2(\tau_6)=\begin{cases}V_2 & \text{if } \tau_6<\tau_3,\\ 0 & \text{if } \tau_3<\tau_6<\tau_4,\\ -V_2 & \text{if } \tau_4<\tau_6,\end{cases}$	$\tau_6=\varphi_{13}+\frac{\alpha_3}{2}$

F. Complete ZVS Expressions

Complete ZVS conditions of TAB depend on the sequence of the switching, as the Thevenin voltage can change in the condition depending on the sequence. This dependence can be illustrated using Fig. 3. It is clear that when calculating the Thevenin equivalent voltage for S2 of port one, v_3 is positive. However, when calculating the Thevenin equivalent voltage, for example, for S7 of port two, v_3 becomes negative. A similar situation can happen to any port, depending on the sequence. Therefore the voltages in the Thevenin equivalent are functions of the sequence of the switching events. Table IV gives a complete overview of the sequences.

1) Non-Linear Parasitic Capacitance $C_{oss,x}$: The C_{oss} is not constant, and it varies with drain-source voltage Vds of the switch in a nonlinear way. As a nonlinear function of V_{ds}, the C_{oss} is usually provided in the datasheet of the power switches. Based on it, the equivalent output capacitance of the switch can be calculated. The derivation of (24) is shown here to demonstrate how the nonlinearity is considered. (24) is obtained by substituting (21) and (22) into (23), which then becomes

$$E_{\text{absorbed}}=2V_{th,x}\int_0^{V_x}C_{oss,x}(v_x)\mathrm{d}v_x=2V_{th,x}\bar{C}_{oss,x}(V_x)V_x \tag{43}$$

where V_x is the dc link voltage of the port where the transistor operates, v_x is the instant voltage of the C_{oss}, $V_{th,x}$ is contant in the discharging procedure. $C_{oss,x}(v_x)$ is provided in the datasheet. The only thing is that the datasheet usually doesn not provide an analytical $C_{oss,x}(v_x)$ but data points of $C_{oss,x}(v_x)$. Thus, curve fitting is needed to get an analytical $C_{oss,x}(v_x)$, which can be submitted to the above equation to obtain $E_{absorbed}$. In the end, $\bar{C}_{oss,x}(V_x)$ as a function of V_x can be calculated as,

$$\bar{C}_{oss,x}(V_x)=\frac{1}{V_x}\int_0^{V_x}C_{oss,x}(v_x)\mathrm{d}v_x \tag{44}$$

As seen, if V_x does not change or have only a slight change, $\bar{C}_{oss,x}(V_x)$ can be considered as constant. In case V_x varies a lot, $\bar{C}_{oss,x}(V_x)$ at different V_x can be calculated beforehand, and a look-up table based on it can be used for online ZVS analysis.

2) Dead-Time: The dead time can influence the ZVS from two aspects: 1. the rising edge or falling edge of the port ac voltage may get delayed due to deadtime. Which edge will be delayed depends on the polarity of the port current at the moment of related leg commutation. This effect will be significant when deadtime is comparable with the switching cycle; 2. ZVS is a procedure of LC resonance. Assuming the converter operates on the boundary of ZVS before the switch turns on, its drain-source voltage will first drop to zero and increase again. So the deadtime must match the resonance time to turn on the switch at the exact time when its drain-source voltage drops to zero. Earlier or later, ZVS can not be achieved. However, this is only valid when the converter is on the boundary of ZVS. If the port current is much larger than

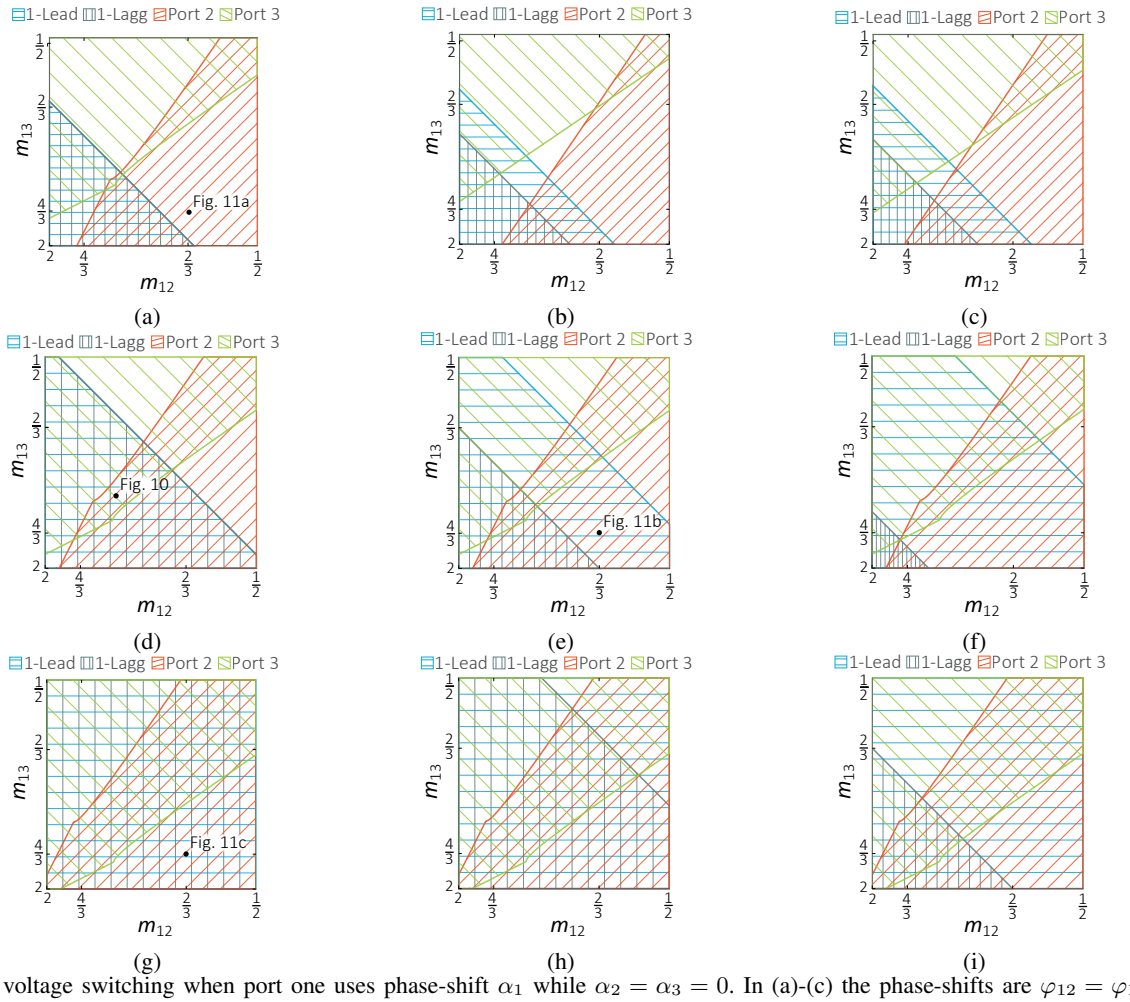


Fig. 6: Zero voltage switching when port one uses phase-shift α_1 while $\alpha_2 = \alpha_3 = 0$. In (a)-(c) the phase-shifts are $\varphi_{12} = \varphi_{13} = 0.05\pi$, in (d)-(f) $\varphi_{12} = \varphi_{13} = 0.15\pi$ and in (g)-(i) $\varphi_{12} = \varphi_{13} = 0.3\pi$. In (a),(d) and (g) phase-shift $\alpha_1 = 0$, in (b),(e) and (h) phase-shift $\alpha_1 = 0.15\pi$ and in (c), (f) and (i) phase-shift $\alpha_1 = 0.45\pi$.

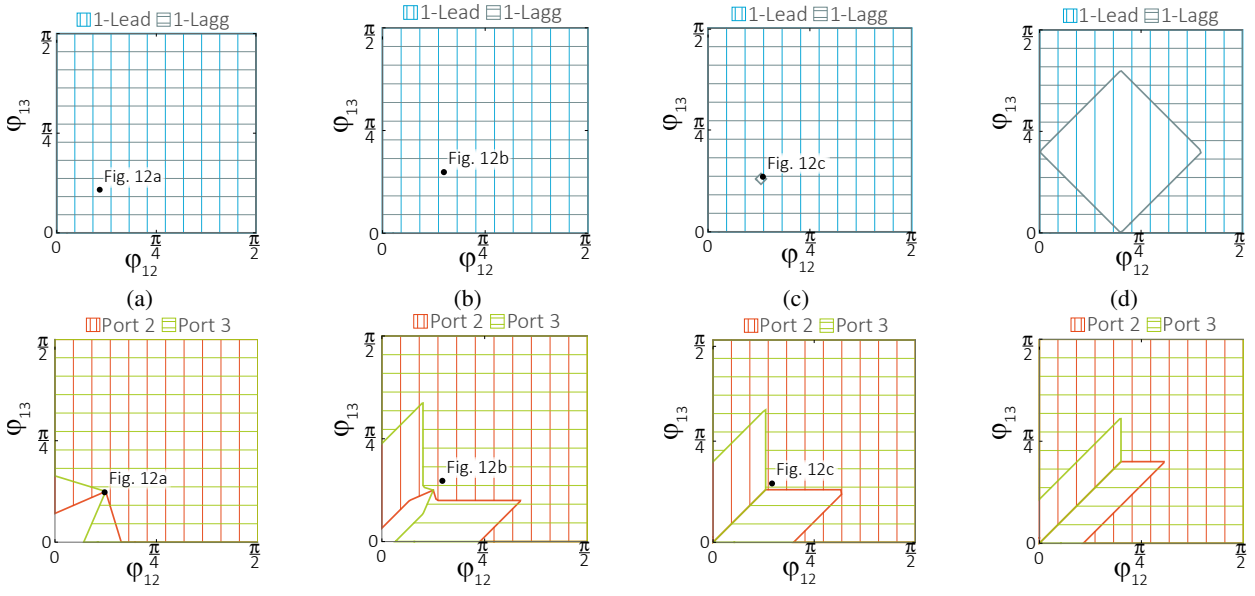


Fig. 7: Calculated zero voltage switching areas when $m_{12} = m_{13} = \frac{4}{3}$. In (a) and (e) $\alpha_1 = 0$. In (b) and (f) $\alpha_1 = 0.2\pi$. In (c) and (g) $\alpha_1 = 0.25\pi$ and in (d) and (h) $\alpha_1 = 0.4\pi$

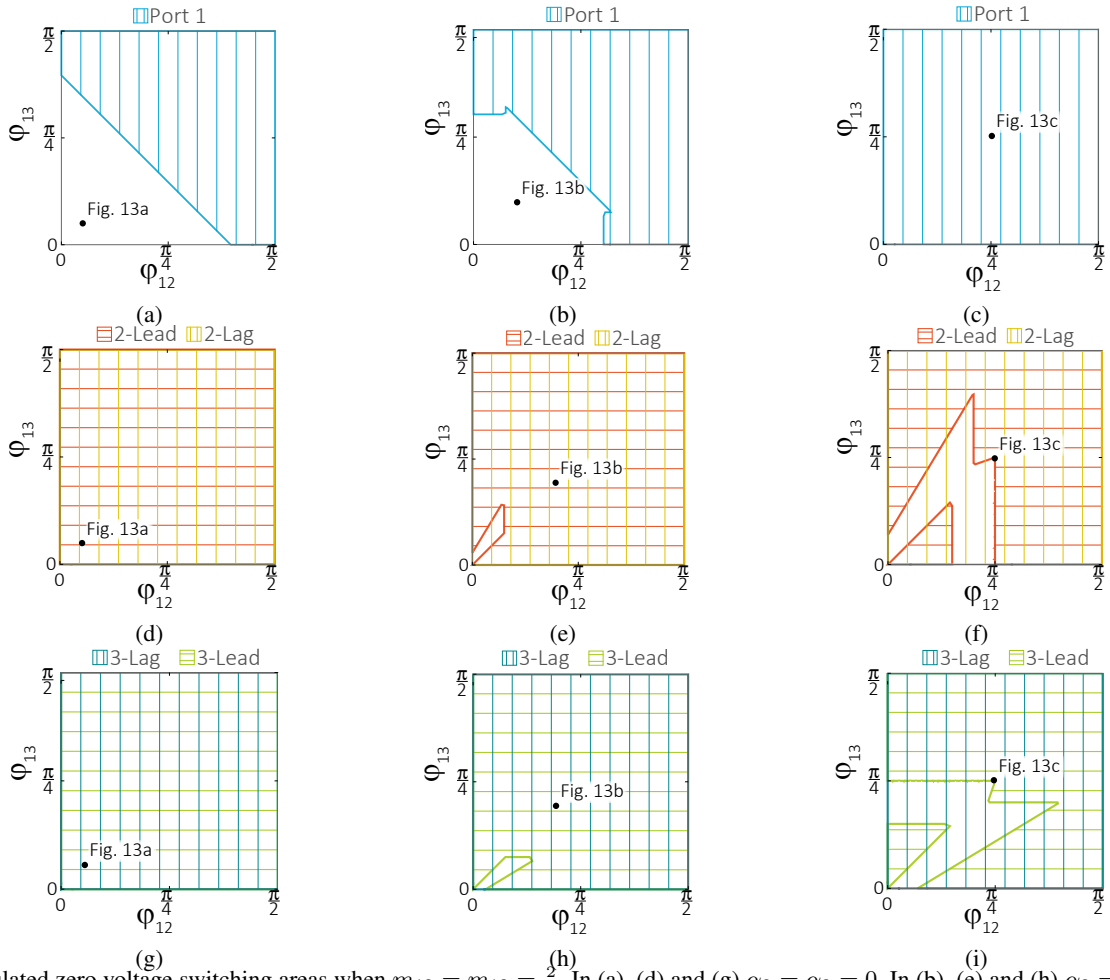


Fig. 8: Calculated zero voltage switching areas when $m_{12} = m_{13} = \frac{2}{3}$. In (a), (d) and (g) $\alpha_2 = \alpha_3 = 0$. In (b), (e) and (h) $\alpha_2 = \alpha_3 = 0.15\pi$. In (c), (f) and (i) $\alpha_2 = \alpha_3 = 0.4\pi$.

the minimum current for ZVS, as long as deadtime is longer than the switch's discharging time, ZVS can be achieved.

G. Soft-switching Analysis

The surfaces were calculated using parameters summarised in Table V. Figure 6 shows the ZVS areas of all three ports as a function of voltage ratios m_{12} and m_{13} when phase-shifts φ_{12}, φ_{13} and α_1 are used while $\alpha_2 = \alpha_3 = 0$. In figures, 1-Lead and 1-Lagg are defined as the leading leg (composed of S_1 and S_2) and lagging leg (composed of S_3 and S_4) of port one; 2-Lead and 2-Lagg are defined as the leading leg (composed of S_5 and S_6) and lagging leg (composed of S_7 and S_8) of port two; 3-Lead and 3-Lagg are defined as the leading leg (composed of S_9 and S_{10}) and lagging leg (composed of S_{11} and S_{12}) of port three. In Fig. 6 phase-shifts φ_{12}, φ_{13} are equal and are varied in the vertical direction, going from 0.05π in the first row to 0.3π in the third row. Phase-shift α_1 is varied in the horizontal direction, i.e., in the first column $\alpha_1 = 0$, while in the third, it is 0.3π. A general observation is that ZVS is achieved at ports with higher voltage, while the ports that have smaller voltage do not achieve ZVS. Moreover, as is the case in the dual active bridge, increasing the phase-shifts φ_{12}, φ_{13} leads to ZVS across the large range of voltage ratios. However, large phase-shifts also mean larger losses due to increased circulating power. Secondly, it is clear that for port one, which is assumed to always lead in Fig. 6, it is, in general, easier to achieve ZVS for the leading phase-leg.

The ZVS areas of all three ports as a function of phase-shifts φ_{12} and φ_{13} when voltage ratios m_{12} and m_{13} are both equal to $\frac{4}{3}$ is shown in Fig. 7. Figure 7 also shows the effect of changing phase-shift α_1. As is clear from the figure, achieving ZVS on port one with the highest voltage is possible across the whole operating region. However, for port two and three, the soft-switching areas are limited. Especially at very light loads achieving ZVS on all phase-legs is difficult. Increasing phase-shift α_1 reduces the ZVS area of the lagging half-bridge in port one. It is interesting to observe the difference between Fig. 7b and Fig. 7c, when even a relatively small difference in phase-shift α_1 leads to loss of soft-switching on the lagging phase-leg of port one. When phase-shift α_1 is increased even further, then soft-switching can be achieved even for very small phase-shifts on port two and three. However, it leads to loss of soft-switching for lagging phase-leg on port one.

The ZVS areas of all three ports as a function of phase-shifts φ_{12} and φ_{13} when voltage ratios m_1 and m_2 are both equal to $\frac{2}{3}$ is shown in Fig. 8. Figure 8 shows the ZVS area

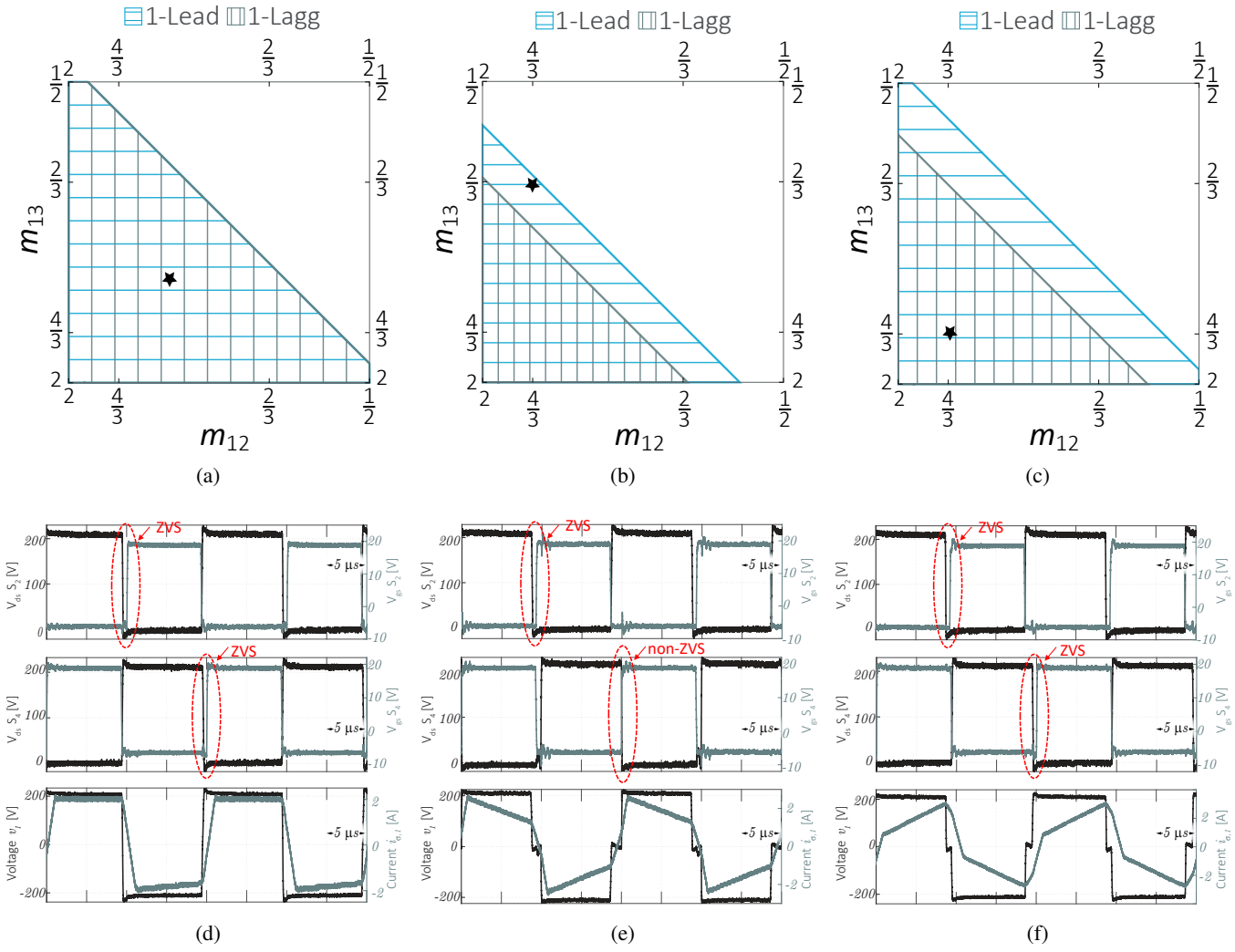


Fig. 9: Calculated zero voltage switching areas of port 1 with: (a) $\alpha_1 = 0$ and $\varphi_{12} = \varphi_{13} = 0.15\pi$; (b) $\alpha_1 = 0.08\pi$ and $\varphi_{12} = \varphi_{13} = 0.1\pi$; and (c) $\alpha_1 = 0.08\pi$ and $\varphi_{12} = \varphi_{13} = 0.2\pi$. The ZVS areas are validated by testing shown in: (d) as a verification of (a); (e) as a verification of (b); (f) as a verification of (c). Note: The operation points of the test in (d) (e) (f) are marked as a star in (a) (b) (c), respectively.

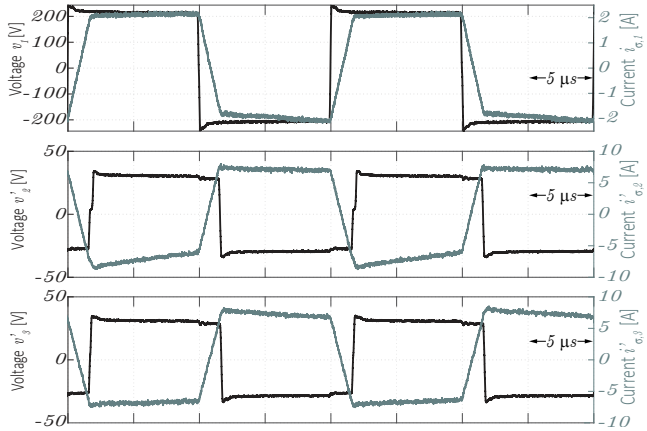
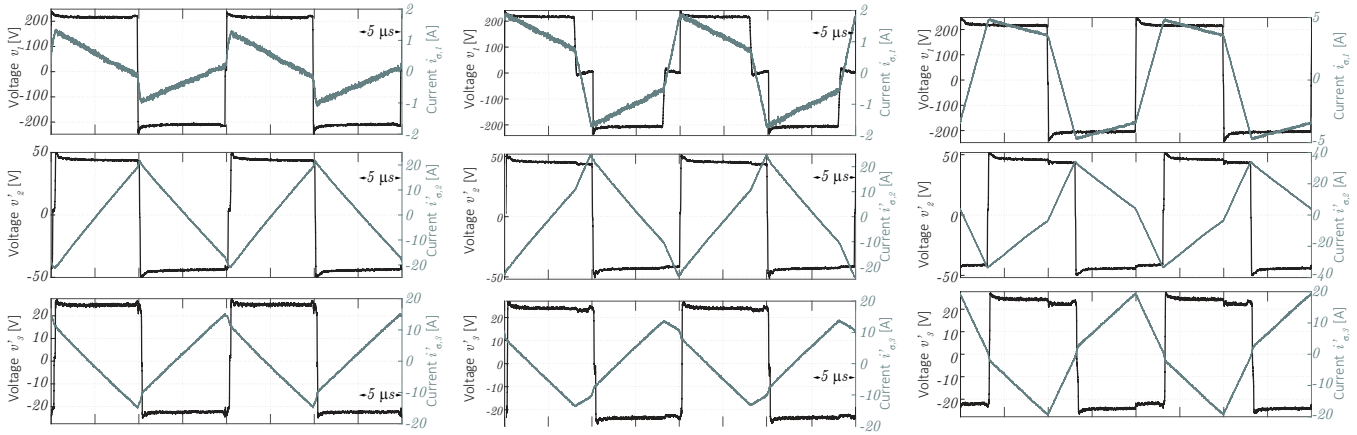


Fig. 10: Operation of TAB converter at unity voltages and all halfbridges achieving ZVS. The phase-shifts φ_{12} and φ_{13} are 0.15π.

for each port separately for better clarity as four out of five degrees of freedom are in use. ZVS is achieved on port one only for relatively large phase-shifts φ_{12} and φ_{13}. Increasing phase-shifts α_2 and α_3 leads to an increase of ZVS area of the port one. However, the cost of achieving ZVS transitions on port one is the loss of soft-switching on the leading phase-leg on ports two and three. The origin of this can be seen in Fig. 3. As is clear, the current needs time to reverse polarity before the lead half-bridge turns on. This time is reduced when phase-shifts α_2 and α_3 are larger than zero. On the contrary, for the lagging half-bridge, this time is increased, thus achieving ZVS for the lagging leg is easier. Moreover, it is clear that achieving ZVS on all ports and all phase-leg simultaneously becomes very difficult when the ports are not loaded equally or have highly unbalanced voltages.

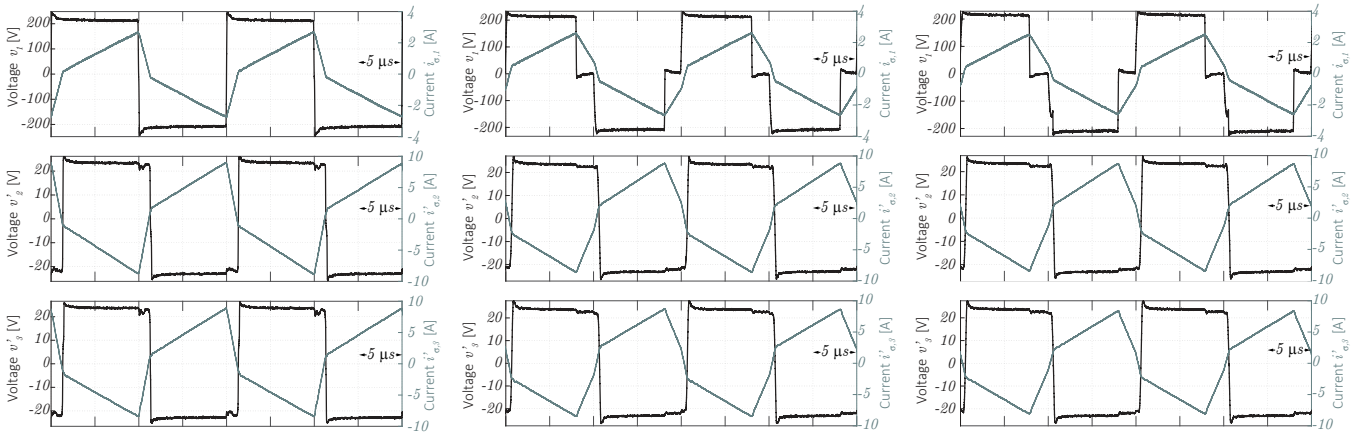
IV. Experiment

A prototype converter has been built to verify the analysis presented in the previous section. The prototype parameters are summarised in Table V. Several operating points were chosen to demonstrate ZVS or hard commutations.



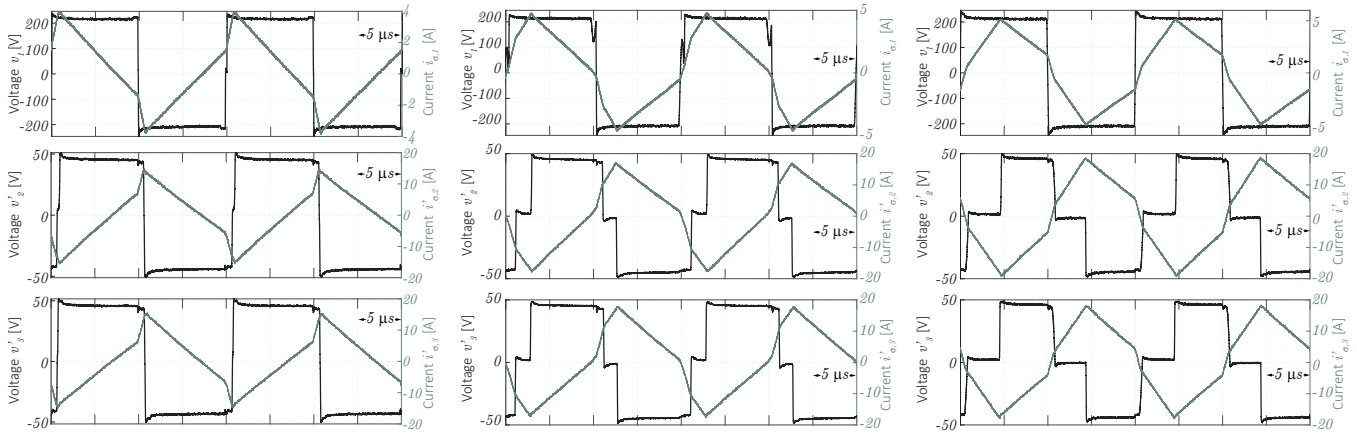
(a) (b) (c)

Fig. 11: Measured commutations of ports when $m_{12} = \frac{2}{3}$ and $m_{13} = \frac{4}{3}$. In (a) $\varphi_{12} = \varphi_{13} = 0.05\pi$. In (b) $\varphi_{12} = \varphi_{13} = 0.15\pi$ and $\alpha_1 = 0.15\pi$. In (c) $\varphi_{12} = \varphi_{13} = 0.3\pi$



(a) (b) (c)

Fig. 12: Measured commutations of ports when voltage ratios $m_{12} = m_{13} = \frac{4}{3}$. In (a) $\varphi_{12} = \varphi_{13} = 0.1\pi$.In (b) $\varphi_{12} = \varphi_{13} = 0.15\pi$ and $\alpha_1 = 0.2\pi$. In (c) $\varphi_{12} = \varphi_{13} = 0.15\pi$ and $\alpha_1 = 0.25\pi$.



(a) (b) (c)

Fig. 13: Measured commutations of ports when voltage ratios $m_{12} = m_{13} = \frac{2}{3}$. In (a) $\varphi_{12} = \varphi_{13} = 0.1\pi$. In (b) $\varphi_{12} = \varphi_{13} = 0.2\pi$ and $\alpha_1 = 0.15\pi$. In (c) $\varphi_{12} = \varphi_{13} = 0.25\pi$ and $\alpha_1 = 0.4\pi$

Since the three ports are symmetrical, showing the ZVS region for one port should cover all the scenarios. Therefore, the analyzed ZVS regions for Port one, shown in Fig. 9 (a)-(c) are verified, and the test results are shown in Fig.9 (d)-(f). The operating points of the test in Fig.9 (d)-(f) are marked in Fig. 9(a)-(c), respectively. The test results show MOSFET drain-source voltage, gate-source voltage, port ac voltage, and current, which can be used to identify whether the two legs of Port one are in ZVS or not. For instance, the test in Fig. 9(e) shows that the leading leg (S2) is in ZVS, while the lagging leg (S4) is out of ZVS, which matches the analysis in Fig. 14(b) very well. Similarly, it can be seen the test results in Fig. 9(d) and (f) also match the analyzed ZVS region in Fig. 9(a) and (c) well.

More tests are done at other operation points, and the operation points are also marked in Fig. 6, Fig. 7 and Fig. 8. First the ZVS operation of the converter when voltage ratios are $\frac{2}{3}$ and $\frac{4}{3}$ for m_{12} and m_{13} respectively are shown in Fig. 11. The operating point shown in Fig. 11a is also marked in Fig. 6a. It is clear that the port with the smallest voltage does not have a soft-switching transition as the current during the transition has the opposite polarity. Similarly, ZVS is not achieved at Port one, as the current is just crossing zero during the commutation. Next operating point is shown in Fig. 11b marked in Fig. 8e. The port with the highest voltage is soft-switched. The port with the smallest voltage is hard-switched, as shown by the current polarity. At Port one, the leading half-bridge achieves ZVS. However, the lagging half-bridge is hard switched as the current changes polarity during phase-shift α_1. The last operating point shown for various voltage ratios is in Fig. 11c and shown in Fig. 6g. As expected, when the phase-shifts are large, even for significantly different voltages, a complete ZVS operation can be achieved on ports two and one. However, the current at Port three is still too small to achieve soft-switching.

Figure 12 confirms the effect of phase-shift α_1 when voltage ratios $m_{12} = m_{13}$ are $\frac{4}{3}$. Figure 12a shows operating point marked in Fig. 7a and Fig. 7e. In the experimental results, the currents are already reversed on all three ports. Figures 7b and 7f mark the operating point measured in Fig. 12b. Port one achieves ZVS, even at the lagging port. Port two and three show that the current had enough time to cross zero before the commutation, and the current is higher at the end of commutation than it was in the previous case, and the ZVS transition is achieved. The last operating point marked in Fig. 7c and Fig. 7g is shown in Fig. 12c. At these operating points, the current at ports two and three had time to change polarity before commutation. However, the current at Port one, when the lagging phase-leg commutates, changes polarity. This leads to a hard transition, thus increasing losses and electromagnetic interference.

Last operating point verified is shown in Fig. 13 when voltage ratios are $m_{12} = m_{13} = \frac{2}{3}$, in this set of experimental results the effect of phase-shifts α_2 and α_3 are verified. Starting with operating point marked in Fig. 8a, 8d, 8g is shown in Fig. 13a where port one does not achieve ZVS as clearly the current has opposite polarity as needed. However, ZVS is smoothly achieved on Port two and three. The effect of introducing phase-shifts α_2 and α_3 is shown in Fig. 13b, this operating point is marked in Fig. 8b, 8e, 8h. It can be observed that the current at Port one is crossing zero during commutation; thus, double transitions are occurring. However, at these operating points, ZVS is kept on all switches on the secondary ports. It is clear why achieving ZVS for the lagging half-bridges on ports two and three are easier than for the leading half-bridges. The current has more time to rise. This effect is even stronger for the operating point shown in Fig. 13c which is marked in Fig. 8c, 8f, 8i. It is possible to achieve ZVS at port one at this operating point as the commutation occurs before the current reverses polarity and no hard commutations occur. However, at ports two and three, it is clear that the current during commutation of the leading half-bridges is still minimal compared to other transitions. The small current amplitude leads to breaking the energy condition and hard transition for the leading half-bridges. On the other hand, the lagging phase-legs undergo soft transitions as the current had enough time to rise.

V. Conclusion

The paper derives the zero voltage switching (ZVS) criteria of the triple active bridge (TAB) converter using Fourier series expansion. Closed-form solutions are summarised and used to investigate the influence of different practical design aspects on the soft-switching regions, including the dc side voltage ratio, the phase shift between ports, and the internal phase shift of each port.

A significant advantage of the derived ZVS criteria is that the effect of parasitic capacitors is considered, ensuring complete commutation of each phase-leg. In general, the port with higher voltage can achieve ZVS easier. Phase shift inside the full bridge can be applied to the port with higher voltage so that the ZVS region of the ports with lower voltage will be enlarged. However, the cost is a reduction of the ZVS region of the port with non-zero internal phase shift, and to be more specific, the ZVS region of its lagging leg if the port is sourcing power, or leading leg if the port is absorbing power. Experiments on a laboratory prototype then verify the closed-form solution of the ZVS and the theoretical analysis. The derived ZVS criteria present a powerful tool to study the operation of TAB converter and further optimisation of its operation. Moreover, the approach outlined in the paper can be generalised to any phase-shift operated n-port topology.

APPENDIX

PROTOTYPE PARAMETERS

TABLE V: Prototype Parameters

Parameter	Acronym	Value
HV MOSFET	S_{1-4}	C3M0030090K
LV MOSFET	S_{5-12}	IPB017N10N5
HV MOSFET Capacitance	$C_{oss,1-4}$	131 [pF]
LV MOSFET Capacitance	$C_{oss,5-12}$	1810 [pF]
Transformer ratio	N	7 [-]
Switching Frequency	f_{sw}	50 [kHz]
Primary Inductance	$L_{\sigma,1}$	106 [μH]
Secondary Inductance	$L_{\sigma,x}$	3 [μH]
Output Capacitance	$C_{out,x,x}$	1.22 [mF]
Primary Resistance	$R_{\sigma,1}$	206 [mΩ]
Secondary Resistance	$R_{\sigma,x}$	22 [mΩ]

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