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We report an atomic layer deposition based zinc oxide channel material integrated thin film transistor using wavy channel architecture allowing expansion of the transistor width in the vertical direction using the fin type features. The experimental devices show area efficiency, higher normalized output current, and relatively lower power consumption compared to the planar architecture. This performance gain is attributed to the increased device width and an enhanced applied electric field due to the architecture when compared to a back gated planar device with the same process conditions. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4836235]

Thin film transistor (TFT) is intended to produce high output current with lower power consumption. Since TFTs used in high resolution and large panel displays are in high demand from the consumers, low-cost integration of TFTs is critical. In accordance with the scaling trend of logic transistors, scaling the TFTs is also a pursued method to increase the output current.[1] However, scaling is expensive, and it also shortens the width of the transistor. Therefore, a fin type feature integrated wavy channel architecture can play critical role to increase the width without increasing the transistor area and consequently can increase the output current.[2] In this letter, we use atomic layer deposition (ALD) based zinc oxide (ZnO) channel material (comparatively low cost oxide material with conformal and uniform deposition feature) to examine the effects of fin aspect ratio and pitch on the output current. In the recent past, semiconductor industry has started to use an advanced non-planar 3D Fin Field Effect Transistor (FinFET) or tri-gate device architecture for tighter electrostatic control over the channel and for mitigated Short Channel Effects (SCEs).[3,4] In these devices charge transport takes place in the fin itself which are typically formed by patterning the substrate itself (most often a silicon-on-insulator substrate). Since we are using thin film based channel material therefore we pattern the substrate to use the fin as a mold for both the gate dielectric and the semiconductor layer in order to achieve an area efficient TFT. Since both channel uniformity and conformity are critical for the performance of our architecture, we used ALD for both of them.[5] We chose ZnO as active material since amorphous oxide semiconductors (AOSs) are desirable for their high mobility, transparency, and low temperature deposition that allows integration on flexible substrates.[6] We also chose high-κ dielectric aluminum oxide (Al_2O_3) as it forms a better interface with ZnO compared to conventional SiO_2.[7]

The process flow to fabricate the wavy channel TFT is as shown in Figs. 1(a)–1(d), where the fin features are first patterned in a heavily doped n-type silicon substrate, with a minimum resistivity of 0.008 Ω cm, which is also used as a back gate. Fin features were etched using Deep Reactive Ion Etching Process (DRIE) process for 6 cycles. The fin height was measured to be 1.5 μm by a profilometer. A planar control sample, without fins, was also processed in parallel with the exact same materials and process conditions and the planar device consumes the same chip area as the fin devices. The fin feature patterning process is followed by deposition of 50 nm of ALD Al_2O_3 at 300 °C. Source and drain of titanium based adhesion layer followed by gold as metal contact (Ti-Au) were then deposited at room temperature by sputtering process and patterned by a lift-off process. Next a low-temperature (100 °C) deposition of ALD ZnO was carried out using 250 ALD cycles.[8] The deposition temperature was optimized to get the desired film resistivity that allows TFT operation. Often higher deposition temperatures lead to higher conductivity in ZnO, hindering effective control of the carrier concentration in the channel via gate modulation. This leads to transistors which turn ON under zero gate bias (depletion mode transistors) and attain low I_{on}/I_{off} ratio.[7] The film resistivity was confirmed by a four-point probe measurement to be ~1 Ω cm. Next, device isolation was carried out by wet etching using diluted HF (H_2O:HF = 25:1) solution for 10 s. A 4 μm thick photoresist was used to protect ZnO active area. Fig. 1(e) shows a 50 μm channel length transistor, with 16 fins. The figure is for a bottom gate bottom contact device, and it shows an overlap area between the ZnO and Ti-Au electrodes.

The planar device has a device width of 250 μm and gate length of 50 μm. In the fin design, as shown in Fig. 1(a), W1 = 4 μm and W2 = 1.5 μm were chosen as the fin width and height, respectively, achieving an aspect ratio of ~3. W3 was varied to vary the number of fins used per-device, and W3 = 4, 8, 12, and 20 μm giving 32, 21, 16, and 10 fins per transistor occupying the same chip area of the planar device. The extra device width, W_{extra}, due to the fin architecture can be calculated as

$$W_{extra} = 2 * W2 * \text{number of fins per device}.$$

This would give W_{extra} of 30, 48, 63, and 96 μm for the fabricated 10, 16, 21, and 32 fin devices, respectively.

A cross sectional scanning electron microscope (SEM) of the ZnO/Ti-Au/Al_2O_3/Si is shown in Fig. 2(a) showing a

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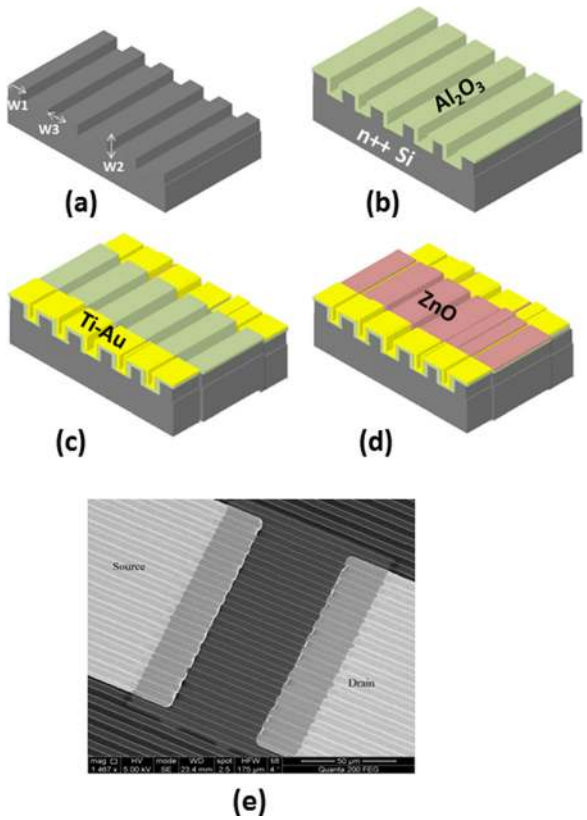

FIG. 1. Process flow for fabrication of fin thin film transistor. (a) We pattern fin features in the heavily doped n-type substrate, where **W1** is the fin width, **W2** is the fin height, and **W3** is the distance between two consecutive fins. This is followed by (b) ALD Deposition of Al_2O_3 gate dielectric, (c) Ti-Au direct current (DC) sputtering of the source and drain and patterning them by lift-off process, and finally (d) deposition of ALD ZnO and device isolation by dilute HF solution. (e) SEM image showing top view of a 16 fin 50 μm channel fabricated TFT.

thickness of ~47 nm of Al_2O_3, 128 nm of Ti-Au layer, and ~40 nm of ZnO, respectively. The films are uniform and conformal without any voids. The SEM image also shows a smooth interface with both the gate dielectric and the source and drain metal pads. The Grazing Incidence X-Ray Diffraction (GIXRD) confirms that the film is mostly amorphous with very weak Wurtzite peaks, as shown in Fig. 2(b), and Fig. 2(c) shows an Atomic Force Microscopic (AFM) image of the ZnO film. The SEM image (Fig. S1 in supplementary material[14]) shows nano-sized grains in ZnO film further confirming GIXRD finding.

The transfer and output characteristics of the planar and wavy channel TFTs are compared and shown in Figs. 3(a) and 3(b), respectively. An early turn-on of the devices as well as an increased drain current is noticed as the number of fins increases. Threshold voltages, V_t, are 6.4, 3.0, 3.8, 2.6, and 2.1 for the planar, 10, 16, 21, and 32 fin devices, respectively. Threshold voltages were extracted using an extrapolation method in the saturation region that determines V_t from the gate voltage axis intercept of the $\sqrt{I_{d\,sat}}$–V_g curve extrapolated at the point of its maximum first derivative, as reported in the literature.[9] They are plotted against the number of fins in Fig. 4(a), where V_t values are shown to decrease linearly as a function of the number of fins. For the drain current, the drain current value for the planar device is comparable to other reports in the literature for ALD based ZnO TFTs.[10–13] As for the drain currents for the fin devices, they are shown also as a function of the number of in Fig. 4(b). The devices have shown a monotonic and linear increase in the drive current as a function of the number of fins showing a 3.7× increase over the planar devices for the same biasing conditions for the drain and gate for the largest number of fins, 32 fins. However, although the devices are showing linear increase of the drain current as a function of the number of fins incorporated, the increase in the drive current cannot be attributed only to the extra device width, W_{extra}, since for the 32 fins based TFT the ratio of the areas of the fin to the planar TFT is ~1.4 while the drain currents ratio is 3.7, for the same biasing conditions as shown in Fig. 4(c). As a result, the I_{on}/I_{off} ratios of the wavy channel TFTs are higher than planar devices, which are of the order of 10^5, considering an off current value of 1 nA for all devices. Finally, we have checked for signs of ZnO channel delamination for wavy channel devices after electrical stressing using SEM imaging, and no signs of delamination or pinholes in the channel were observed. We have added this image as Fig. S2 supplementary material.[14]

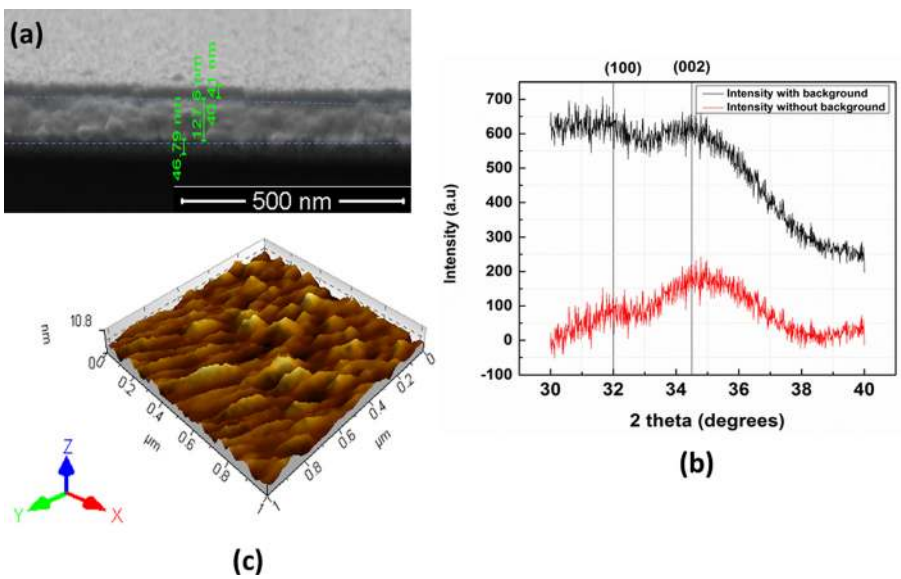

FIG. 2. (a) Cross sectional SEM showing the thicknesses (top to bottom) of the ZnO, Ti-Au, and Al_2O_3 layers; (b) grazing incidence XRD with and without background, showing very weak peaks and proving the amorphous nature of ZnO; and (c) an AFM image showing root mean square (RMS) roughness of 1.5 nm.

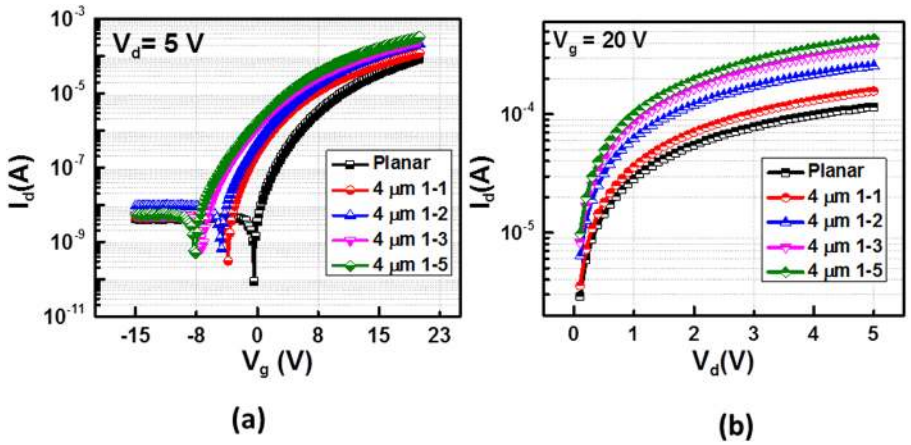

FIG. 3. (a) Transfer and (b) output characteristics comparison between fin TFTs and planar transistor all-consuming the same chip area. The convention for naming fin devices is $W1$ 1: $\frac{W3}{W1}$. So 4 μm 1:1 is a 4 μm wide fin with 4 μm distance between every two consecutive fins.

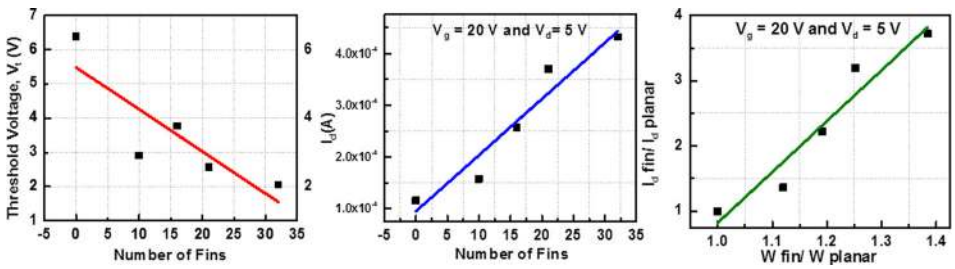

FIG. 4. (a) Threshold voltage, V_t, variation as a function of the number of fins with linear fit added to the data points. (b) Drain current as a function of the number of fins at the $V_g = 20$ V and $V_d = 5$ V. (c) Fin to planar drain current ratio as a function of fin to planar device width ratio.

The increased device current can be explained on an enhanced electric field effect. In Fig. 5, the electric field lines around corners show an enhanced field due to field components from both the side walls of the fins and the planar part.

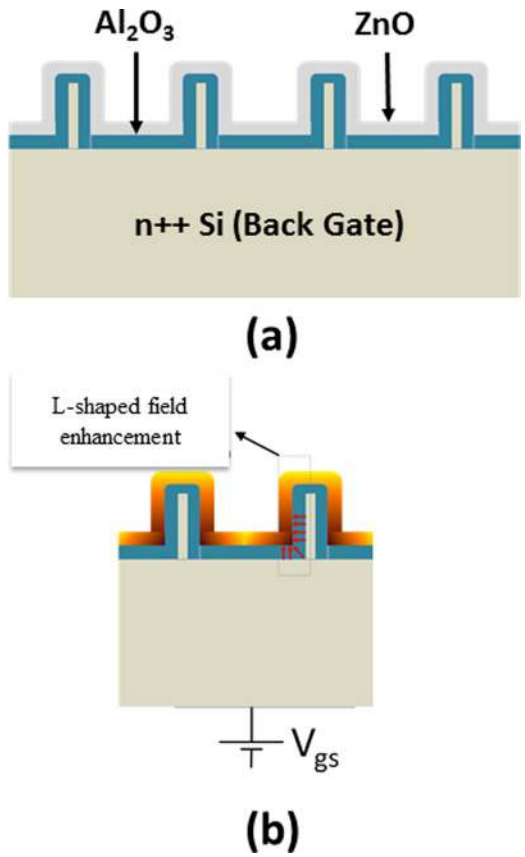

FIG. 5. Fin devices at (a) no bias and (b) with bias showing an enhancement in the applied field at corners due to contribution from both the side walls and the planar part, which is termed L-shaped field enhancement.

We give this the term L-shaped field enhancement. This has been manifested in the devices as the threshold voltage decreased as a function of the number of fins as was shown in Fig. 4(a). To confirm our hypothesis, we have studied the current improvement for larger width, smaller aspect ratio: 16 μm fins. Consistent results were found confirming that current improvement could be explained based on L-shaped field enhancement effect and suggesting that a higher current could be achieved using larger number of fins, or higher aspect ratio fins. We added the 16 μm fins electrical characteristics to Figures S3 and S4 in supplementary material.[14] The L-shaped field enhancement effect allows operation at lower voltages since control over the threshold voltage is possible through variation of the number of fins. This is advantageous since the threshold voltage can be tailored using the fin architecture to suit the operating voltage. That could also lead to more energy efficient since power consumption is lower when lower operating voltage (V_{dd}) is used as power consumption (P) is quadratically proportional to the operating voltage: P α V_{dd}^2. This would allow the TFT to be integrated in applications that require low V_{dd} such as active matrix organic light emitting diode (AMOLED) based screens for cell phones.

In conclusion, we have shown that wavy channel architecture thin film transistor allows expansion of device width in the vertical direction using the fin architecture. This architecture also allows the control over the threshold voltage as a function of the number of fins, which helps to tailor the TFT for lower operating voltages. The maximum number of fins device has shown a 3.7× increase of drive current over the planar counterpart consuming the same chip area. The enhancement was shown to be a linear function of the number of fins and cannot be attributed only to the extra vertical device width. An enhanced electric field effect is shown due to edges, namely, the L-shaped field enhancement. This could explain the earlier turn on of the devices as a function

of the number of fins. Future work should examine fins of smaller fin width and larger fin height to examine their effects on both the drive current and switching behavior.

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[14]See supplementary material at http://dx.doi.org/10.1063/1.4836235 for the pictorial depiction of the SEM images of the ZnO wavy channel transistor, no delamination in ZnO film, electrical characteristics supporting the hypothesis of L-shaped field enhancement.