Zooming in on Network-on-Chip Architectures

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Abstract. The aim of this talk is to expose the theoretical distributed system community to the concept of Network-on-Chip (NoC), an emerging research field within the VLSI realm, in which networking principles play a significant role, and new network architectures are being explored in a new setup as well as new cost and performance models. Researchers should find new challenges in exploring solutions to familiar problems such as network design, routing, and quality-of-service, in unfamiliar settings under new constraints. The unique characteristics of silicon chips require new solutions to these classical problems, and define a new set of NoC specific problems, such as automatic network design process, power and area optimization and specialized system functionalities.

We present a new classification of chip architectures into three categories with different requirements from their NoCs. In order to stimulate some research directions, we highlight several research problems arising in these categories such as routing, quality-of-service, flow and congestion control, and resource allocation (e.g., capacity assignment, sharing hot-spots). We provide initial solution directions to example problems.

S. Kutten and J. Žerovnik (Eds.): SIROCCO 2009, LNCS 5869, p. 1, 2010.