ZPUC: A New Configuration of Single DC Source for Modular Multilevel Converter Applications

SAEED ARAZM (Student Member, IEEE), AND **KAMAL AL-HADDAD** (Fellow, IEEE)

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École de technologie supérieure, University of Quebec, Montreal, QC H3C 1K3, Canada

CORRESPONDING AUTHOR: SAEED ARAZM (e-mail: saeed.arazm.1@ens.etsmtl.ca).

ABSTRACT Z packed U-cell (ZPUC) converter topology is presented in this paper as a new type of multilevel converter topology that can be operated in a single phase as well as in three-phase configurations while using a single DC source. Since each U-cell includes two switches and one capacitor, in this topology, three U-cells are needed to generate 5 or 7 voltage levels. Moreover, the configuration proposed for the ZPUC is more appropriate for high-power application modular multilevel converters (MMCs) to increase the voltage levels compared to other topologies. Accurate voltage balancing on small-sized auxiliary capacitors is due to integrated modulation strategy without using additional controllers; additionally, the reduction of total harmonic distortion (THD) in AC currents for higher voltage levels is an advantage of this configuration. A full topology sequence of operation and performance analysis of ZPUC based on the 5-L inverter is investigated in Matlab-Simulink and experimentally validated on a 3 kVA prototype. The obtained results illustrate the good dynamic performance of the proposed topology and the implemented integrated switching pattern voltage balancing.

INDEX TERMS ZPUC topology, modular multilevel converter (MMC), ZPUC-MMC active voltage balancing, power quality, reliability.

I. INTRODUCTION

Multilevel converter topologies have become more popular and are progressively replacing two-level converters due to their high impacted advantages on reducing the size of harmonic filters, increased nominal power capability and component voltage stress reduction [1]. Cascaded full bridge, flying Capacitor (FC), neutral point clamped (NPC) and active neutral point clamped (ANPC) are the popular and classic topologies of multilevel converters that have been commercialized in recent years, replacing conventional converters in several industrial applications [2]–[5].

Multilevel converters have recently been used in medium-voltage and high-voltage applications, such as medium-voltage drives , the connection of solar and wind turbine plants to the main grid, and high-voltage direct current (HVDC) and flexible AC transmission systems (FACTS) [6], [7].

Multilevel converters present many challenges related to isolated DC sources [8], topology complexity [9], modulation techniques [10], modeling and control [11], as well as the voltage balancing challenge [12] of flying capacitors that have persuaded researchers and industries to improve and enhance their performance.

Modular multilevel converters (MMCs) have become attractive to industries in recent years for their modularity, which is vital for repair and maintenance due to simple exchange of the affected modules by new ones. Other advantages that have contributed to MMCs' growing popularity include voltage scalability, lower total harmonic distortion (THD), higher quality of output voltage and current waveforms, fault tolerance, and redundancy [13], [14]. Reducing the power losses in semiconductor switches and the sizes of filters are the other useful features of MMCs [15], [16].

With regard to the impacts of the increased number of devices, assembling complexity, heat dissipation of losses, and total cost of the multilevel converters and MMCs, the tendency nowadays is to develop multilevel converter topologies with reduced numbers of power devices while generating more voltage levels.

Multilevel submodules such as 3-L NPC, 5-L FC, 3-L full bridge, 5-L cross-connected cells and 3-L FC are the blocks that can be replaced by 2-L usual half bridge on MMCs to counteract its negative effects [17], [18]. However, to have an optimized topology of MMCs, considering their application as well as the standard requirements, would be necessary in order to trade off between the complexity of cells and power losses. In addition, higher output voltage levels accompanied by proper modulation techniques make the harmonic filters smaller due to the reduced THD of the output wave [19], [20].

Recently several new topologies of multilevel converters were proposed based on hybrid FC, NPC and CHB topologies with the aim of increasing the voltage levels and reducing the component counts. A reduced component count five level converter was presented in [21]. However, it uses the common FC topology for three-phase which has an impact on system reliability when used in three-phase configuration and in case of one phase failure. The authors proposed 5-L topologies in [22] for open end induction motor (OEIM) applications with the aim of increasing the reliability and fault tolerance. Although this topology, solve the reliability problem, its application is limited for OEIM. In [23] a single-phase Seven-Level Inverter for reduced components count was proposed; however, the latter requires three isolated DC sources for three-phase system. In [24] authors present a new seven level topology in which single DC source has been replaced by an isolated DC source. A new approach to voltage level multiplication has been introduced that permits the multiplication of the number of output voltages while operating at different frequencies to enhance converter efficiency [25].

Packed U-cell (PUC) topology is one of the recently introduced topologies of multilevel converters that highly reduces the component count [26]. This converter generates seven voltage levels through six switches three of which operate complementarily. Thus, there is no redundancy, which requires the complicated control system to balance the auxiliary capacitor [27]. The authors in [28] utilized the redundancy in PUC and achieved five voltage levels at the output wave while the FC was controlled without sensors and only by a modulation technique. In [29], [30] modulation techniques were presented to control PUC5 without any sensors as well. Moreover, authors in [31] present nine levels waveform through an additional U-cell that is called PUC9 and voltage balancing method to balance two FCs. More recently, several papers have been published for modification of PUC converter. In [32], a nine level T-type PUC is presented which generate nine levels at the output of inverter; however, it uses two DC source for single-phase converter. Authors present an improved PUC topology as a boost converter which makes the output AC voltage peak of inverter up to one and half times of input

voltage [33]. However, this topology uses three additional switching devices compared to traditional PUC converter.

It is worth noting that all the literatures which has already been published regarding PUC converters, require isolated DC sources in a three-phase system which is their main drawback. To cope with this challenge of isolated bidirectional power flow DC sources, a new topology is presented in this paper called Z packed U-cell (ZPUC).

The number of switches in this topology is the same as in PUC; however, one more capacitor has to be added in order to replace the bidirectional DC source in standard PUC.

ZPUC topology can be extended through additional U-cells, and the output voltage levels would be increased to two times minus one for redundant states and two-times plus one for non-redundant states in terms of adding one U-cell. The simplest module of ZPUC includes three U-cells which generates five levels with redundant switching states that are easily controlled and seven levels with an added complex control system. ZPUC can generate 9-L for redundant switching states and 15-L for non-redundant switching states, just by adding one more U-cell. The number of devices in ZPUC topology is very low in comparison with the other topologies such as FC and NPC. It should be noted that one of the major advantages of this new topology is that it requires only a single DC source for all systems configuration such as single-phase, three-phase, and multiphase connections as well. The voltage levels generated by proposed topology are unipolar that are instrumental to operate as a single DC source to generate higher voltage levels compared to a bipolar one such as PUC converter.

In this paper the new topology of ZPUC and the switching states for single-phase and three-phase system is discussed in Section II. As well, voltage balancing algorithm integrated with modulation technique and reliability is discussed in this section for one sub-module of ZPUC. The application of ZPUC5 on MMCs are discussed in Section III. Finally, Simulations and experimental results are shown in Section IV and V for stand-alone and grid-connected aimed to validate the performance of ZPUC single phase and three phases which implement voltage balancing technique.

II. ZPUC TOPOLOGY AND SWITCHING STATES

The simplest model of ZPUC topology that has been shown in Fig. 1(a) has six switches same as PUC5 in which three devices works complimentarily. Thus, there are eight states for this topology that generate 5-L waveform with regard to necessary redundancy to balance the voltage in the flying capacitors or 7-L with complex control system. Additional flying capacitor can be added to make this topology appropriate for generating more voltage levels especially in a three-phase system with a single DC source. In fact, an additional capacitor in ZPUC5 compared to PUC5 makes the output waveform unipolar at E step from 0 to 4E instead of −2E to +2E in PUC converter. Generation of unipolar waveform at the output of ZPUC topology makes this topology suitable to generate more voltage levels in MMC configuration in comparison with the
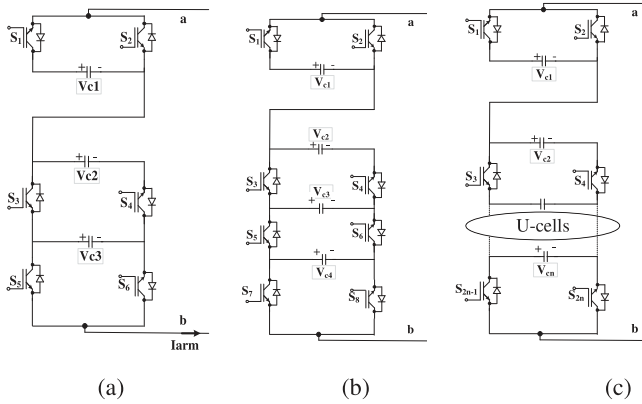
FIGURE 1. (a) Simplest ZPUC converter topology with three capacitors and 6 switches that can generate 5-L or 7-L waveform, (b) ZPUC9 or ZPUC15 topology, and (c) General model of ZPUC.

TABLE 1. Switching States of ZPUC Converter to Generate Five And Seven Level Waveform

State	S1	S3	S5	Vab	Vab-5L	Vab-7L
1	1	0	0	Vc1+Vc2	4E	6E
2	1	0	1	Vc1+Vc2 −Vc3	3E	5E
3	1	1	0	Vc1+ Vc3	3E	4E
4	1	1	1	Vc1	2E	3E
5	0	0	0	Vc2	2E	3E
6	0	0	1	Vc2 −Vc3	E	2E
7	0	1	0	Vc3	E	E
8	0	1	1	0	0	0

PUC topology. Fig. 1(b) shows that one U-cell and one FC has been added to simplest ZPUC which output voltage levels are increased by two-times minus one for redundant states (9-Level) and two-times plus one (15-L) for non-redundant states. Fig. 1(c) shows the general topology of ZPUC. The relation between the U-cells and voltage levels is given by equations 1 and 2.

$$M = 2^n + 1 \tag{1}$$

$$M = 2^n - 1 \tag{2}$$

Where n is the number of U-cells, and M is the voltage levels. Eq. (1) and 2 are relevant for redundant switching states and nonredundant switching states, respectively.

A. SWITCHING STATES OF ZPUC5

There are six active switches in simplest ZPUC inverter which switches S_1, S_3 and S_5 operate in complimentary way with S_2, S_4 and S_6 respectively. Eight switching states in this topology generate 5 voltage levels at the output with sufficient redundancy to balance the voltage in flying capacitors. This topology uses the redundant states to balance the voltages without complicated control system and only through modulation strategy. Equation (3) and (4) show the relation between the states and the output voltage levels. Eq. (3) is related to the simplest ZPUC that could generate 5-L or 7-L depend on the relation of V_{C1}, V_{C2}, and V_{C3}. Furthermore, Eq. (4) is applied for general type of ZPUC proposed topology.

$$V_{ab} = S_1 V_{c1} + (1 - S_3)V_{c2} + (S_3 - S_5)V_{c3} \tag{3}$$

$$V_{ab} = S_1 V_{c1} + (1 - S_3)V_{c2} + (S_3 - S_5)V_{c3}$$
$$+ \ldots \ldots (S_{2n-3} - S_{2n-1})V_{cn} \tag{4}$$

Where V_{ab} is the output voltage across nodes ab in Fig. 1, V_{c1}, V_{c2}, V_{c3}, and V_{cn} are the flying capacitor voltages in C_1, C_2, C_3 and C_n respectively and S_1, S_3, S_5 and S_{2n-1} are the switching devices that would be 1 when the switches are turned on and would be 0 when they are turned off. Simplest

ZPUC switching states is listed in the Table 1 according to equation 3 and their corresponding topologies are depicted in Fig. 2. In order to generate 5-L voltage across ab node (V_{ab}), voltages in capacitors 1 and 2 (V_{c1} and V_{c2}) should be regulated in 2E and voltage in capacitor 3 (V_{c3}) must be regulated in E which is illustrated in Eq. (5). Accordingly, to generate 7-L waveform across the ab node the voltages should be set as the Eq. (6).

$$V_{C1} = V_{C2} = 2E, V_{C3} = E \tag{5}$$

$$V_{C1} = V_{C2} = 3E, V_{C3} = E \tag{6}$$

In Fig. 3 the inverter model of ZPUC topology is depicted which could be operated as a single DC source single-phase or three-phase multilevel inverter. As well, additional modules could be easily added in series connection which is suitable for MMC applications. In next section the performance of ZPUC for MMC is discussed.

This configuration is suitable for industrial applications such as motor drives, renewable energy connection to the grid, HVDC etc. Voltage waveform across the load in Fig. 3 includes 9-L for phase voltage and 17-L for line voltage. ZPUC converter topology has been devised so that it could be placed in all applications of converters such as active rectifier and multilevel inverter and is much suitable for application on modular multilevel rectifier and inverters as well as the excellent candidate to replace the half bridge or full bridge used till now as a unique cell for MMC application. As well, capability of this converter to balance the flying capacitor voltages integrated with modulation technique and without using the external control system in desired values with minimum ripples and offset would be interesting for industries. This topology requires the single DC source for three-phase system in contrast with the other competitive topology such as the PUC. The value of this topology is the reduced counts of power devices than the other equivalent topologies such as NPC, FC, and CHB to generate equal voltage levels at the output [19], [34], [35].

Table 2 shows the comparison among the number of devices in several popular type of inverters in three-phase systems to generate 9-L phase-waveform and 17-L line waveform.
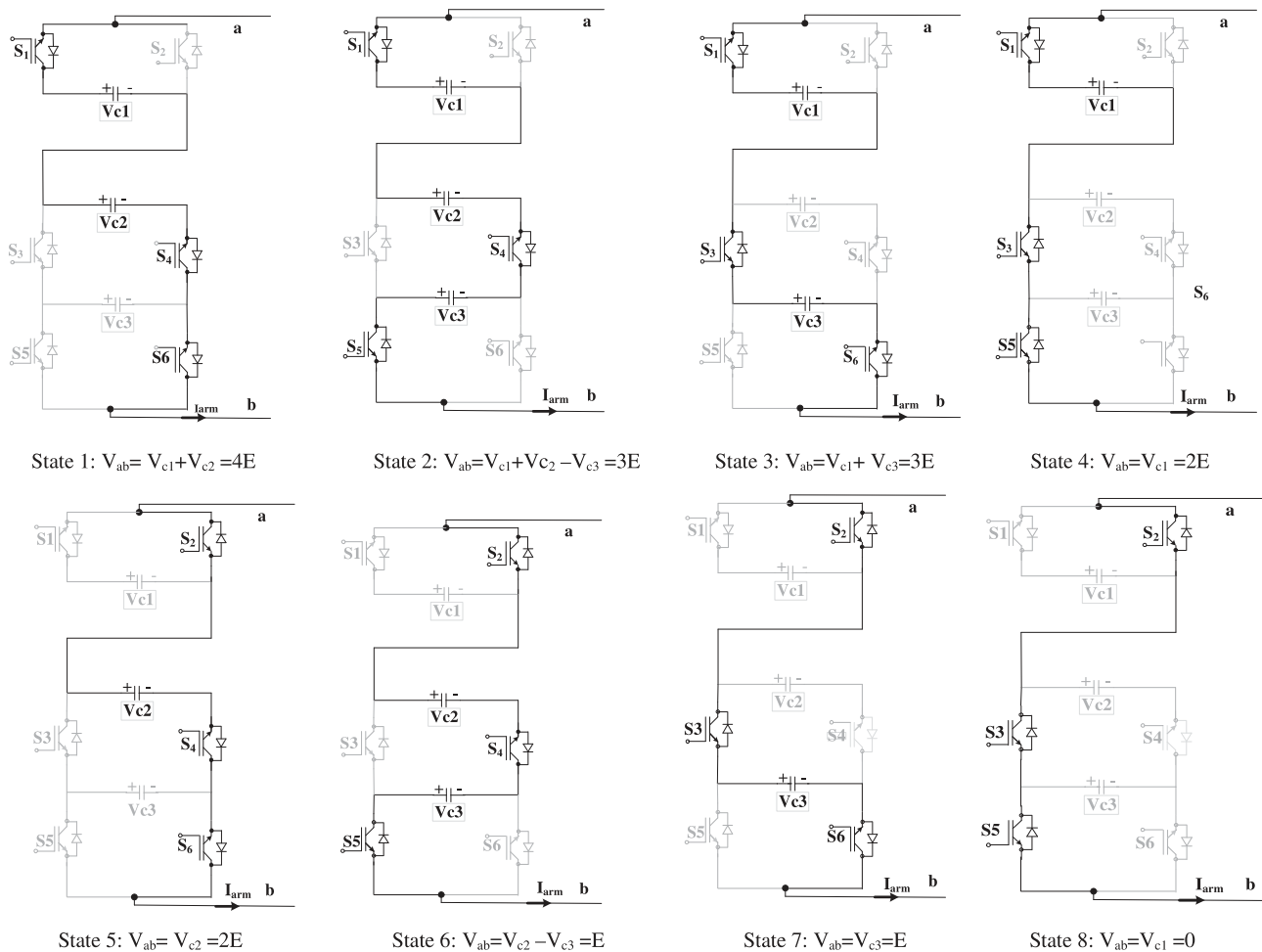
State 1: $V_{ab} = V_{c1} + V_{c2} = 4E$

State 2: $V_{ab} = V_{c1} + V_{c2} - V_{c3} = 3E$

State 3: $V_{ab} = V_{c1} + V_{c3} = 3E$

State 4: $V_{ab} = V_{c1} = 2E$

State 5: $V_{ab} = V_{c2} = 2E$

State 6: $V_{ab} = V_{c2} - V_{c3} = E$

State 7: $V_{ab} = V_{c3} = E$

State 8: $V_{ab} = V_{c1} = 0$

FIGURE 2. Switching states of ZPUC inverter in standalone mode.

TABLE 2. Components Counts of Three-Phase Inverters to Generate 9-L Phase Voltage Wave

Inverter Type	DC Source	Capacitor	Clamped Diode	Active Switch	Total components
CHB	12	0	0	48	60
NPC	1	8	42	48	99
FC	1	21	0	48	60
PUC5	6	6	0	36	48
PUC9	3	6	0	24	33
ZPUC5	1	18	0	36	55

This table illustrates that the number of switching devices in ZPUC is less than the other type of converters and is equal to the PUC5. However, the number of isolated DC sources in ZPUC5 is 1/6th of PUC5 that could be a suitable alternative for PUC5 in three-phase systems due to the considerable cost and bulkiness reduction of DC supply system and complexity. It is noteworthy that, ZPUC topology is not only suitable converter for three-phase system due to single-DC source requirement, but also for single-phase application compared to other PUC family of converters. For instance, single-phase traditional PUC5 converter requires two isolated DC sources

and 12 switches and two FCs to generate 9-L waveform in contrast to the single DC source, 12 switches, and 6 FCs for ZPUC converter. Although ZPUC5 requires 4 more FCs, the cost of isolated DC sources is still an issue. PUC9 is the converter that uses three DC sources with lower number of switching devices; however, this topology is not as modular as ZPUC and it could not be suitable for higher levels waveforms in three phase applications.

In addition, a general ZPUC topology that can be replaced in all Poles as to increase the voltage levels known as the general topology as depicted in Fig. 1(c).

The number of U-cells determine the required total amount of output voltage levels depend on the application. However, to generate more voltage levels; more complex and challenging control and modulation technique and hardware implementation can be expected. To overcome this problem, the authors suggest using the simplest ZPUC5 in modular way which not only, divide the voltages among capacitors and reduce the rating size of elements, but also, would have the other advantages of MMCs.

For designing power converters, dividing the currents between modules is an advantageous way to choose lower current rating switching devices and consequently lower
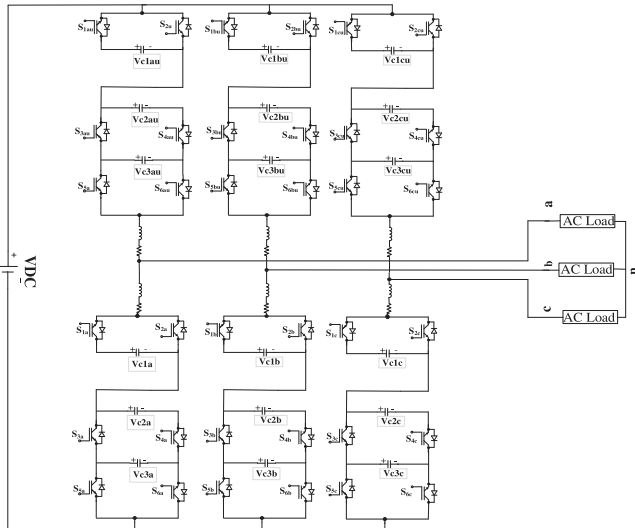
FIGURE 3. Three phase ZPUC converter topology which generates 9-L single phase waveform and 17-L line-voltage waveform.

conduction power losses. This benefit is achieved by the configuration of the Fig. 3, while the voltage levels have been duplicated compared to the other competitive topologies.

B. VOLTAGE BALANCING METHOD ON SINGLE MODULE OF ZPUC5

The theory of voltage balancing in this paper is based on energy storage in each capacitor. With the assumption that capacitance of FCs are similar, measured FCs voltages should be compared with one another in voltage balancing algorithm as a first step. Modulation strategy must be implemented on the converter to generate the appropriate gate signals. Redundant switching states which has been shown in Fig. 2, facilitate to balance the voltage between the involved FCs in each voltage level. If the current flows from the positive polarity of capacitors, it means that the capacitor is being charged and vice versa. Hence, charge and discharge of the FCs depend on the arm current direction and this situation is altered through current direction variation reciprocally. Generally, the FCs with the greater voltage values are selected to be discharged between the redundant states in each voltage level. Situations of charge and discharge of the FCs in terms of current direction (I_{arm}) are listed in Table 3. It should be explained that - sign in the Table 3 demonstrates that the corresponding capacitors are neither charged nor discharged. In other words, they have no effect in the circuit. In addition, abbreviations of CH and DC imply charge and discharge of FCs.

For instance, states 6 and 7 are redundant states which generate voltage level of E at the output of ZPUC module in which capacitors C_2 and C_3 are charged and discharged respectively in state 6, and C_3 is discharged in state 7 when the arm current is positive as shown in Fig. 2. Thus, state 6 must be selected in voltage balancing algorithm to generate E

TABLE 3. Situations of Charging and Discharging of Flying Capacitors at Corresponding States

State	$I_{arm}>0$			$I_{arm}<0$		
	C1	C2	C3	C1	C2	C3
1	CH	CH	-	DC	DC	-
2	CH	CH	DC	DC	DC	CH
3	CH	-	CH	DC		DC
4	CH	-	-	DC		-
5	-	CH	-	-	DC	-
6	-	CH	DC	-	DC	CH
7	-	-	CH	-	-	DC
8	-	-	-	-	-	-

TABLE 4. Voltage Balancing Algorithm for ZPUC of Fig. 2

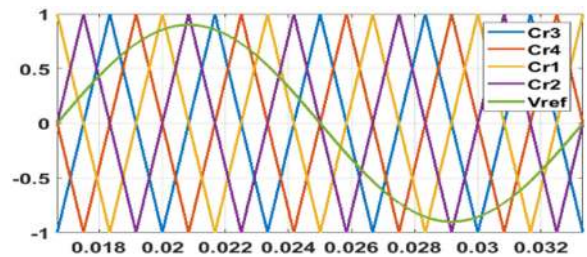| Condition	$I_{arm}>0$	$I_{arm}<0$	Voltage level from modulation strategy
No condition	State1	State1	4E
Vc3>0.5Vc2	State2	State3	3E
Vc3<0.5Vc2	State3	State2	3E
Vc1>vc2	State5	State4	2E
Vc1<Vc2	State4	State5	2E
Vc3>0.5Vc2	State6	State7	E
Vc3<0.5Vc2	State7	State6	E
No condition	State8	State8	0

FIGURE 4. Carriers and voltage reference for modulation of one module of ZPUC.

voltage level in positive arm current when measured voltage value of C_3 is greater than C_2. Inversely, state 7 should be selected between states 6 and 7 when the voltage of C_3 is lower than C_2 at the same arm current direction. Charge and discharge of FCs are reversed when the arm current direction (I_{arm}) is inversed.

The voltage balancing algorithm for one module of ZPUC converter are listed in Table 4 according to above-mentioned explanation.

Phase shift modulation technique introduced in [19] is utilized in this paper. Four carriers and one reference voltage for one module of ZPUC is shown in Fig. 4 and the voltage balancing control method integrated with PS-PWM technique is illustrated in flowchart of Fig. 5. Corresponding states of voltage levels are selected based on comparison between carrier waves and reference voltage. Only the modulation conditions based on the flowchart of Fig. 5 should be investigated to generate voltages of 0 and 4E. Whereas, to generate the other voltage levels including 3E, 2E and E the conditions of
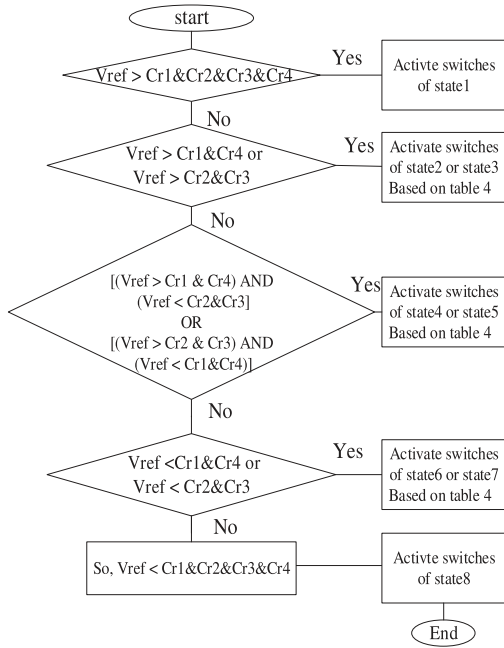
FIGURE 5. Flowchart of voltage balancing integrated with phase-shift modulation strategy.

FIGURE 6. (a) Structure of one module of ZPUC topology based on separated Cells, and (b) reliability block diagram of one module of ZPUC without redundancy and with redundancy.

modulation of Fig. 5 and conditions of voltage balancing of the Table 4 should be examined simultaneously.

C. RELIABILITY OF ONE MODULE OF ZPUC TOPOLOGY

In this section, the reliability of single-phase ZPUC topology is briefly discussed based on the method presented in [36], [37]. As defined, reliability is the performance of the system during a defined time. Based on the IEEE std 493–2007, reliability is the capability of a system to accomplish associated functions over a time [38]. In other words, reliability is the probability that the system functions in its normal operation in defined duration. Its simplified equation is given by [37], [38]:

$$R(t) = e^{-\lambda t} \quad (7)$$

$$\lambda = \frac{1}{MTTF} \quad (8)$$

Where R(t) is the reliability of the system and λ is the failure rating that is an inverse of MTTF (mean time to failure). MTTF shows the time duration in which the equipment or system operates in normal function. Each device or systems in power converters have their own failure rating which are normally mentioned in the manufacturer data sheets. Redundancy would enhance the reliability of the system through reduction in λ index. Two popular series and parallel reliability models has been introduced in [36], [37]. While, there are redundancy in parallel model and operation of k devices out of n devices are adequate for normal operation of system. Total failure rating and reliability in series model is obtained by:
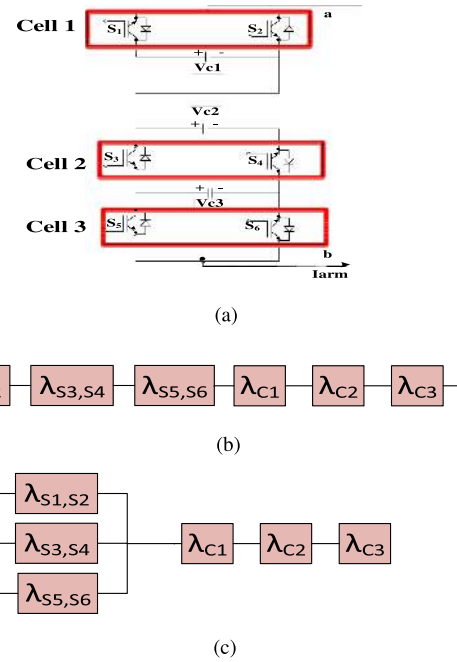
$$\lambda = \sum_{i=1}^{n} \lambda_i \quad (9)$$

$$R(t) = \prod_{i=1}^{n} R_i(t) \quad (10)$$

Where, i denotes the number of devices or subsystems and λ_i is the failure rating of ith subsystem. In non-redundant systems, the reliability is reduced when the devices are added. To illustrate, the topology and reliability block diagram of one module of ZPUC5 topology in series model in which generating 5L waveform is necessary to meet the power quality standard is depicted in Fig. 6(a) and (b). Total reliability of the system for this series model is obtained as Eq. (9) and Eq. (10). In this diagram, $\lambda_{S1, S2}$, $\lambda_{S3, S4}$ and $\lambda_{S5, S6}$ are called failure rating of cell 1, cell 2 and cell 3 respectively. On the other hand, overall reliability of the parallel model for operation of k subsystem out of n subsystem or devices is given by Eq. (11):

$$R(t) = \sum_{i=k}^{n} C(n, i) R_i(t)^i (1 - R_i(t))^{n-i} \quad (11)$$

Where $C(n, i)$ is combination of i elements from a set of n devices or subsystems which is obtained by Eq. (12).

$$C(n, i) = \frac{n!}{i!(n-i)!} \quad (12)$$

Reliability block diagram for one module of ZPUC topology by taking into account the redundancy is illustrated in Fig. 6(c).

One module of ZPUC5 topology generates 5L waveform in normal condition and it generates 4L and 3L when one cell out of three cells is faulty. It also can operate to generate two level waveforms when two cells out of three cells are failed. Thus, depend on the desired voltage waveform at the output of the converter, the reliability of ZPUC module varies due to variation in required redundancy. For instance, combinations of (3, 2) from Eq. (12) must be replaced in equation (11) to obtain the reliability of the ZPUC converter regarding several combinations such as 5L, 4L and 3L output waveform. Following redundancy could be considered for ZPUC module due to failure of cells:

a) normal condition (5L)
b) Cell 1 fails (3L)
c) Cell 2 fails (3L)
d) Cell3 fails (4L)
e) Cells 1, 2 fail (2L)
f) Cells 2, 3 fail (2L)
g) Cells 1, 3 fail (2L)

Reliability for four states from (a) to (d) to have at least 3L waveform in terms of ZPUC module is obtained by summation of reliabilities in these four states by substituting of suitable combination of n from k in Eq. (11). Ergo, the reliability of ZPUC could be increased through redundant states which is another advantage of this topology due to its proper redundancy to generate variety of voltage levels by failing one or two cells out of 3 cells. It also should be noted that to calculate the reliability of converter, the failure rating of controller, gate drives and DC sources must be added to the switching devices and capacitors.

D. VOLTAGE BALANCING METHOD ON THREE-PHASE ZPUC MULTILEVEL CONVERTER

ZPUC converter which is shown in Fig. 3 generates 9L waveform across the load in stand-alone mode. Hence, 8 carrier is required to modulate the reference wave. Fig. 4 shows the carriers Cr1 to Cr4 which are placed in 0°, 90°, 180°, 270° and they are modulated with reference voltage Msin(ωt). These carriers and reference voltage are utilized to build 5-L waveform and voltage balancing in three flying capacitors of the upper arm. As well, carriers Cr5 to Cr8 with -Msin(ωt) which is shown in Fig. 7, are used to balance the voltage and making 5-L voltage in the lower arm. Phase shift among carriers Cr5, Cr6, Cr7 and Cr8 are in 45°, 135°, 225° and 315°. It should be noted that flowchart of Fig. 5 and Table 4 is used for upper and lower arm separately except that the carriers Cr1 to Cr4 must be replaced by Cr5 to Cr8 for lower arm. Control diagram of ZPUC converter which has been shown in of Fig. 3 is depicted in Fig. 8.

To illustrate the algorithm of voltage balancing in ZPUC converter and generation of 9-L waveform, one single line diagram of two ZPUC modules is depicted in Fig. 9.
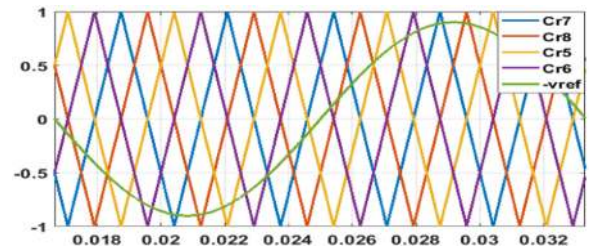

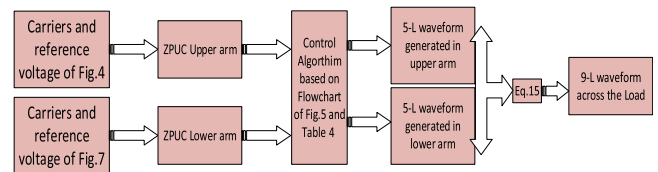**FIGURE 7.** Carriers and voltage reference for modulation ZPUC module of the lower arm shown in Fig. 3.

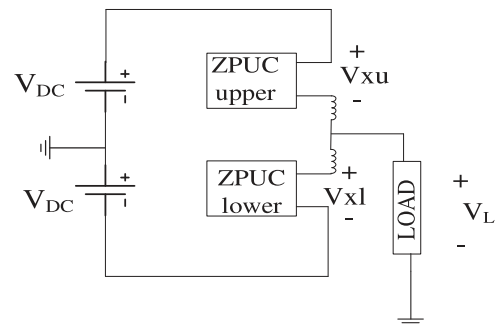**FIGURE 8.** Control diagram of two ZPUC module in 9-L multilevel converter.

FIGURE 9. Single line diagram of 9-L ZPUC converter.

The equations for output voltage of Fig. 9 is given by:

$$V_{xu} = V_{DC} - V_L \tag{13}$$

$$V_{xl} = V_{DC} + V_L \tag{14}$$

$$V_L = \frac{V_{xl} - V_{xu}}{2} \tag{15}$$

V_{xu} and V_{xl} in Fig. 9 are voltages in upper and lower arms, V_L is the load voltage and x index shows the phases a, b, c. Equation 15 shows that load voltage levels would be twice of voltage of each arm so that they sorted in both negative and positive side through mentioned modulation. In other words, 5-L unipolar waveform is produced in upper and lower arms and 9-L bipolar waveform is generated across the load. The control diagram to generate 9-L waveform through voltage balancing integrated with the modulation technique is shown in Fig. 8.

Fig. 10 shows the 9L voltage across the load from ZPUC converter in which 400 V DC voltage is divided in 9 steps having 15.67% voltage THD and 0.9% current THD.
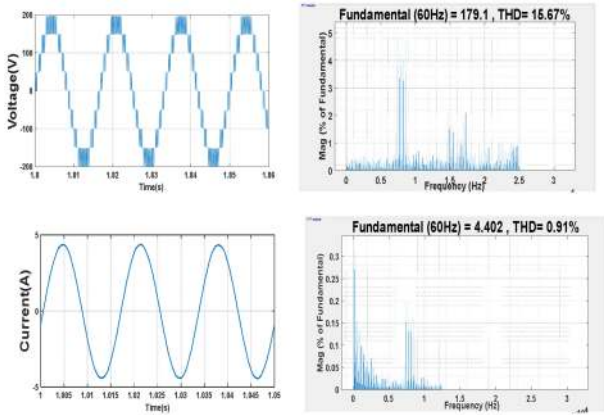
FIGURE 10. Voltage and Current waveform, voltage and current THD of single-phase ZPUC of Fig. 3.
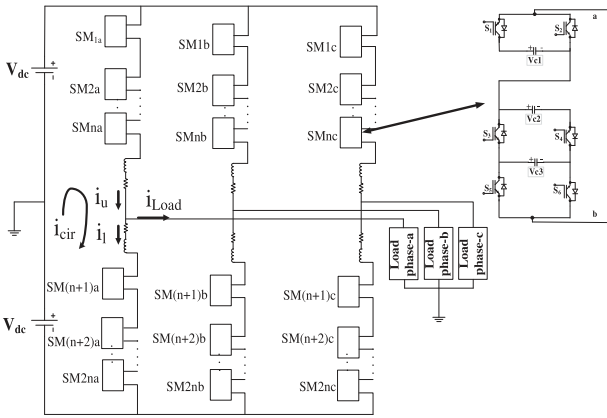

FIGURE 11. MMC configuration with ZPUC submodule.

It should be noted that the total harmonic distortion (THD) on ZPUC multilevel converter is reduced due to increased voltage levels in comparison with the competitive topologies of multilevel converters.

III. APPLICATION OF ZPUC5 ON MODULAR MULTI-LEVEL CONVERTERS (MMCS)

Fig. 11 illustrates the configuration of MMC with sub-module of ZPUC in which MMC configuration consists of cascaded ZPUC in two arms per phase.

Generally, $4N + 1$ levels waveform is generated in upper and lower arm in terms of N submodules in each arm. They are arranged from 0 to 4NE in E steps. It should be noted that 4NE is equal to total DC link voltage or $2V_{DC}$. Load voltage level is equal to $8N + 1$ that is located from $-2NE$ to $+2NE$ in steps ½E. Fig. 12 shows that how voltages are generated in upper and lower arms and accordingly across the load in ZPUC-MMC. Number of voltage levels in ZPUC-MMC is as follows:

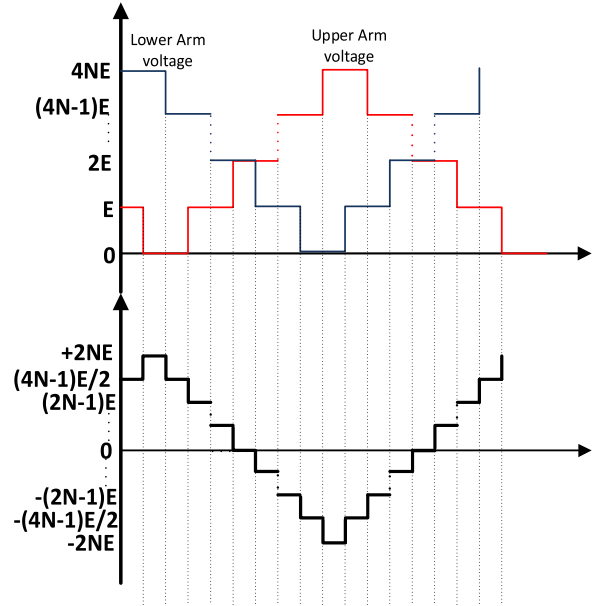$$M_{\text{phase}} = 8N + 1 \qquad (16)$$

FIGURE 12. General voltage waveforms of upper and lower arms and across the load on ZPUC-MMC.

Where M_{phase} is the voltage levels across the load in general ZPUC-MMC. General relation between the line waveform and phase waveform is given by:

$$L_{\text{line}-W} = 2L_{\text{phase}-W} - 1 \qquad (17)$$

Ergo, in ZPUC-MMC the line waveform level across the three-phase loads is obtained by Eq. (10).

$$M_{\text{line}} = 16N + 1 \qquad (18)$$

Following steps shows the algorithm of voltage balancing in MMC based on algorithms listed in Table 4 and flowchart of Fig. 5.

1) Sorting of the total stored energy of each module based on normalized measured voltages of flying capacitors in descending way. The simplified equation with the assumption that all capacitors are similar is as follows:

$$E_{\text{ci}} = \sum_{j=1}^{3} V_{\text{cij}}^2$$

$$I = sort(E_{\text{ci}}) \qquad (19)$$

Where E_{ci} is the total storage energy in ith module of ZPUC in each arm. I is the sorting matrix in which ZPUC modules of each arm are arranged with a maximum energy values to minimum. V_{cij} is the measured voltage of FCs in ith module and j defines the number of capacitors in each module.

a) implementation of modulation strategy to generate voltage levels.

b) defining the direction of corresponding arm current

c) To generate maximum voltage level of 4NE, all submodules per arm should be operated in state 1 based on

TABLE 5. V_{diff} in Corresponding Lower and Upper Arms Voltages

Total Voltage at lower arm ($\sum U_{li}$)	Total Voltage at upper arm ($\sum U_{ui}$)	MMC Output voltage	Difference voltage (V_{diff})
4NE	0	2NE	0
4NE	E	(4N-1)E/2	-E
(4N-1)E	0	(4N-1)E/2	+E
(4N-1)E	E	(2N-1)E	0
(4N-1)E	2E	(4N-3)E/2	-E
(4N-2)E	E	(4N-3)E/2	+E
(4N-2)E	2E	2(N-1)E	0
(4N-2)E	3E	(4N-5)E/2	-E
(4N-3)E	2E	(4N-5)E/2	+E
(4N-3)E	3E	(2N-3)E	0
(4N-3)E	4E	(4N-7)E/2	-E
⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮
4E	(4N-3)E	-(4N-7)E/2	-E
3E	(4N-3)E	-(2N-3)E	0
2E	(4N-3)E	-(4N-5)E/2	+E
3E	(4N-2)E	-(4N-5)E/2	-E
2E	(4N-2)E	-2(N-1)E	0
E	(4N-2)E	-(4N-3)E/2	+E
2E	(4N-1)E	-(4N-3)E/2	-E
E	(4N-1)E	-(2N-1)E	0
0	(4N-1)E	-(4N-1)E/2	+E
E	4NE	-(4N-1)E/2	-E
0	4NE	-2NE	0

*note: $4NE = 2V_{dc}$.

Table 4. To generate voltage level of $(4N − 1)E$, the module corresponding to the first array I (1) in equation (19) should be selected to operate in states 2 or 3. I(1) defines the submodule with the maximum energy which must be selected in order to discharge its FC with the aim of energy reduction. The algorithm described in Table 4 should be used for selection between mentioned states. Actually, the other submodules operate at state 1. As well, to generate state $(4N − 2)E$, the submodules corresponding to the arrays of I (1), I (2) have to be selected to operate in states 2 or 3 depends on normalized voltages as in Table 4. This method is performed for the other voltage levels.

Equation (15) is rewritten by following equation for output voltage of ZPUC-MMC.

$$V_L = \frac{\sum_{i=1}^{N} u_{li} - \sum_{i=1}^{N} u_{ui}}{2} \tag{20}$$

Where, $\sum u_{ui}$ and $\sum u_{li}$ are the total voltage of ZPUC submodules in upper and lower arms. N is the number of ZPUC submodules in each arm and i index implies voltage at the ith ZPUC. Output voltage of ZPUC-MMC with the assumption that $2V_{dc} = 4NE$, is listed in Table 5 based on Fig. 12. The rows of this table show the total voltages on lower arms, upper arms, and output of ZPUC-MMC for corresponding switching states for $8N + 1$ switching states.

A. CIRCULATING CURRENT IN ZPUC-MMC

Circulating current is an issue which appear in modular multilevel converters and increases the power losses due to negative sequence components. Although, it is limited through current limiting inductor that is called buffer inductor, control method also plays the effective role to mitigate and suppress it. Load current and circulating current in terms of upper and lower currents which has been shown in Fig. 11 are obtained by Eq. (21) to (23)

$$i_u - i_l = i_{Load} \tag{21}$$

$$i_{cir} = i_u - \frac{i_{Load}}{2} = i_l + \frac{i_{Load}}{2} \tag{22}$$

$$\frac{i_u + i_l}{2} = i_{cir} \tag{23}$$

Where i_u, i_l and i_{cir} are upper arm current, lower arm current and circulating current respectively. Fig. 11 demonstrates that the circulating current is created through the difference between AC and DC voltages. Following equation is obtained by KVL loop which cause the circulating current in Fig. 11.

$$\sum_{i=1}^{N} (u_{ui} + u_{li}) + L_{arm} \frac{d}{dt} (i_u + i_l) + R_{arm} (i_u + i_l) = 2V_{dc} \tag{24}$$

Where u_{ui}, u_{li} are the output voltage of each submodule in upper arm and lower arm respectively, L_{arm} and R_{arm} are the inductance and resistance of current limiting reactor or buffer inductor and N is number of ZPUC submodules per arm. Regarding to the lower resistance compared to inductance in buffer inductor, the resistance term is neglected from Eq. (24). Moreover, by substituting Eq. (23) into Eq. (24), and separating current terms from voltage terms following equations are obtained:

$$2V_{dc} - \sum_{i=1}^{N} (u_{ui} + u_{li}) = 2L_{arm} \frac{di_{cir}}{dt} \tag{25}$$

$$V_{diff} = 2V_{dc} - \sum_{i=1}^{N} (u_{ui} + u_{li}) \tag{26}$$

Left hand term of Eq. (25) implies the reason why the circulating current is created in MMCs which is shown separately by Eq. (26). In fact, the control method should reduce the difference between the DC voltage and AC voltage to mitigate the circulating current. Although, the buffer inductance, L_{arm}, plays an evident role based on Eq. (25) to mitigate the circulating current, it could not be selected so large due to its bulkiness and much cost of the converter. Circulating current is automatically controlled by proposed voltage balancing control method integrated with modulation strategy through selection of appropriate switching states in upper and lower arm submodules. To illustrate, the difference voltage which cause the circulating current are listed in Table 5 together with ZPUC-MMC arms voltages and output voltage for all $8N + 1$ states. For instance, to generate voltage 2NE at the output of MMC, corresponding switching states should be designated in upper and lower arms to generate voltage levels 0 and 4NE respectively in which difference voltage would be zero according to Eq. (26) and this assumption that $2V_{dc} = 4NE$.

Table 5 shows that the absolute value of voltage difference in all states are zero or E which makes this converter controllable against the circulating current. With regard that DC link voltage, $2V_{dc}$, is assumed to be 4NE, V_{diff} is reduced by increasing the number of ZPUC submodules. In other words, the value of E is reduced through expansion of the submodules due to the following equation:

$$E = \frac{V_{dc}}{2N} \qquad (27)$$

Where V_{dc} is half of the DC link voltage as shown in Fig. 11, E is the step voltage value in the output waveform, and N is the number of ZPUC submodules in each arm. In fact, E parameter in ZPUC-MMC is reduced by increasing the N which demonstrates that Vdiff is reduced as shown in Table 5. Accordingly, the circulating current of ZPUC-MMC is reduced, similarly of DC link voltage by expansion of submodules.

The special control methods to suppress the circulating current could also be implemented on ZPUC-MMC as the other well-known MMCs such as HB-MMC.

B. POWER LOSSES ON ZPUC-MMC

Conduction and switching losses are the main parts of power losses in power converters devices. Conduction loss is created due to the on resistance and on state voltage of switching devices and antiparallel diodes. Switching losses are the loss of energy which are created for nonideality in switches commutation caused by turn on and turn of times. In this subsection, ZPUC converter is compared to the HB-MMC which is the most popular type of MMC in research area and industry, to evaluate from power loss aspect. The power losses have been calculated through presented methods on papers [39], [40]. The calculations have been carried out for the same type of IGBT from Fuji electric (FGW35N60HD).

Following equation can be obtained according to the typical output characteristic figure in manufacturer datasheet for maximum junction operation temperature.

$$i_c = 0.028V_{CE} + 0.933$$
$$i_D = 0.03V_D + 0.9 \qquad (28)$$

Where, V_{CE} is the collector-emitter voltage of IGBT, V_D is the antiparallel diode voltage, i_c is the collector current, and i_D is the antiparallel diode current. Resistance and on state voltage of IGBT and diode are utilized to obtain the conduction losses.

Table 6 shows the parameters of load and DC source that is selected to compare the power losses between two MMCs in the similar primary conditions and the same switching devices. It should be noted that the similar condition is considered to calculate the power losses for two types of MMCs. It can be observed that the total power losses in ZPUC-MMC is lower than. well-known HB-MMC to generate the same voltage levels.

TABLE 6. Power Losses Comparison Between HB-MMC and ZPUC-MMC With 9-L Output Waveform

Parameters	HB-MMC	ZPUC-MMC
Cells per arm	8	1
Vdc (V)	400	400
L_{arm} (mH)	1	1
R_{arm} (Ω)	0.1	0.1
L_{load} (mH)	25	25
R_{load} (Ω)	20	20
Cosφ	0.9	0.9
carrier frequency	2000 Hz	2000 Hz
Modulation Index	0.95	0.95
P	730	730
Q	345	345
Total Power losses	78.2watt	46.87 watt
efficiency	89.43%	93.76%

C. FLYING CAPACITOR DESIGN

Design of flying capacitors in ZPUC converter which consists of three FCs in each module plays a crucial role to mitigate the voltage ripple and consequently to improve the voltage and current waveform. Since, the converters during the grid connected must meet the related standards requirements, FC must be designed carefully in terms of voltage ripple. Following general equation which implies the capacitor current with respect to the capacitance and capacitor voltage is utilized to design the FCs.

$$i_p = C\frac{dv}{dt} = C\frac{\Delta v}{\Delta t} \qquad (29)$$

Where, i_p is the peak of the load current, C is the capacitance of FCs in ZPUC converter, Δv is the peak to peak voltage ripple which can be selected based on permissible value in associated applications. As FCs of ZPUC modules operate at switching frequency in the proposed voltage balancing control method, capacitance value of FCs is obtained by Eq. (30).

$$C = \frac{i_p}{f_{sw}\Delta v} \qquad (30)$$

Where f_{sw} is the switching frequency.

For instance, C on the ZPUC converter set up of Fig. 3 with DC source of 100V is 2000μF which based on the switching frequency of 1000 Hz and load current peak of 2A, voltage ripple on the lower FCs are 1 V. With regard that voltage on the lower capacitor should be regulated on 25 V, voltage ripple is 4%. Capacitance value can be selected lower with increasing the permissible voltage ripple or increase on the DC source voltage. On the other hand, it should be selected in higher value when load current increases.

D. GRID CONNECTED MODE OF ZPUC-MMC

ZPUC converter could also be operated as an inverter to inject the current into the grid. Voltage balancing control in this mode is exactly as explained in stand-alone mode. However, current control must be carried out in grid connected mode to protect the converter against the overcurrent which cause the failure of devices. Furthermore, the power factor is controlled while the power is injected to the grid. Fig. 13 shows the
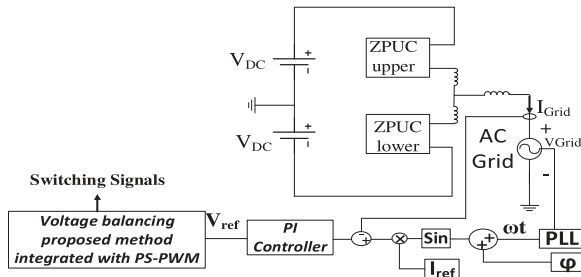
FIGURE 13. Single-line diagram of controller for ZPUC converter in grid connected mode.

TABLE 7. Simulation and Experimental Parameters of Stand-Alone Mode

DC source voltage	100 V
Switching frequency	1000 Hz
System frequency	60Hz
Load	40 Ω, 20 mH
Buffer inductance	2 mH
Capacitor C1, C2, C3	2000 μF
Sampling time	46 μs

FIGURE 14. 9L phase voltages and 17L line voltages in three-phase single DC source ZPUC inverter.

FIGURE 15. Three-phase current and current THD of ZPUC converter.

single-line diagram of control for ZPUC converter in grid connected mode.

Typical PI controller is used to show the performance of ZPUC converter in grid connected mode. I_{ref} $Sin(\omega t + \varphi)$ is the reference current that is the desired injected current into the grid in which phase angle, ωt, is obtained by PLL circuit. I_{ref} is the current amplitude which is adjusted based on the power rating of converter to restrain the overcurrent and to preserve the converter in case of fault events.

Injected current from ZPUC inverter into the grid is measured and then it is subtracted by reference signal to generate the error signal. Output of PI controller makes the voltage reference signal from the error current signal that is sent to the modulation strategy integrated with the voltage balancing program to balance the flying capacitor voltages and to control the grid current simultaneously. Through appropriate selection of phase shift, φ, the desired value of power factor is achieved which could be a profitable option for connection of photovoltaic power plant to the grid. Moreover, this converter could play the role of active and reactive power compensator through regulating of phase shift when it works in grid-connected mode. The associated results are discussed in results section to show the performance of the converter on grid connected mode.

IV. SIMULATION RESULTS
The proposed converter has been studied by simulation using MATLAB/Simulink on standalone feeding RL loads and grid connected system in order to verify the proposed topology operation as well as the proposed control method on ZPUC-MMC. The system parameters which has been used in simulation and experimental stand-alone tests are listed in Table 7.
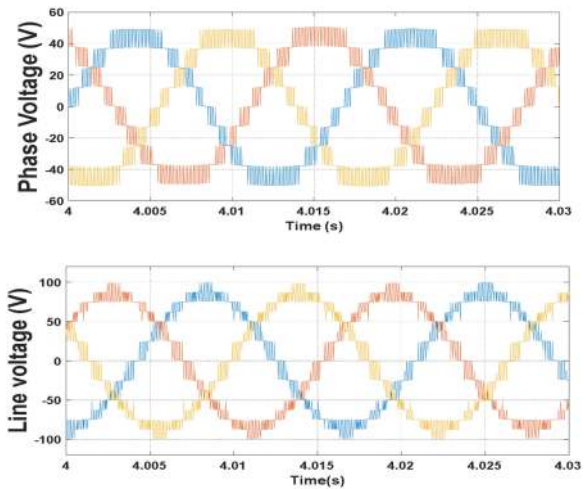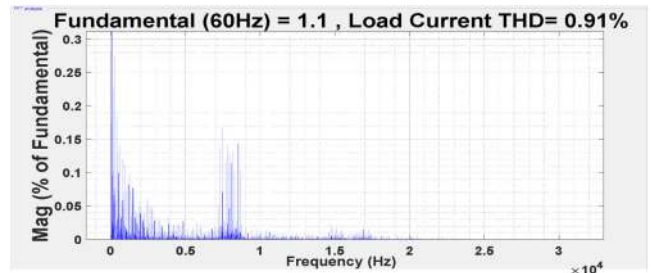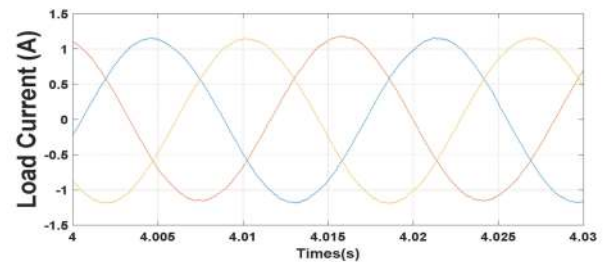
Voltage balancing algorithm integrated with phase shift PWM method [19] is used to show the voltage balancing in flying capacitors in this case study.

A. STANDALONE MODE
Nine level phase voltage and seventeen level line voltage across the three-phase star load of single DC source three-phase ZPUC converter of Fig. 3 is shown in Fig. 14. Moreover, Fig. 15 shows the three-phase current and related THD in steady state which demonstrate the performance of this converter and proposed voltage balancing integrated with modulation technique.
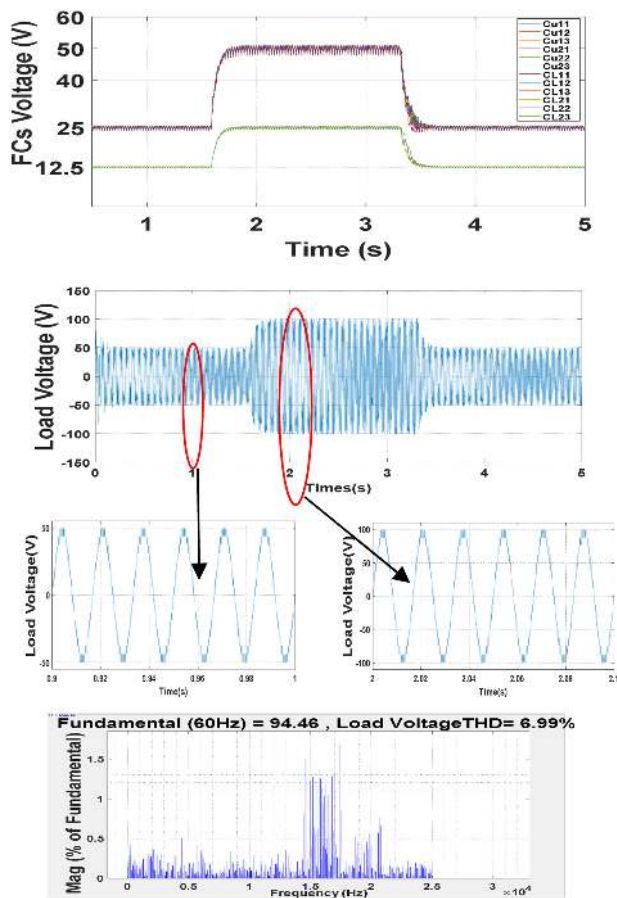
FIGURE 16. FCs voltage waveforms and load voltage during the DC link variation from 100 V to 200 V and back to 100 V, Load voltage THD when the DC link has been increased.
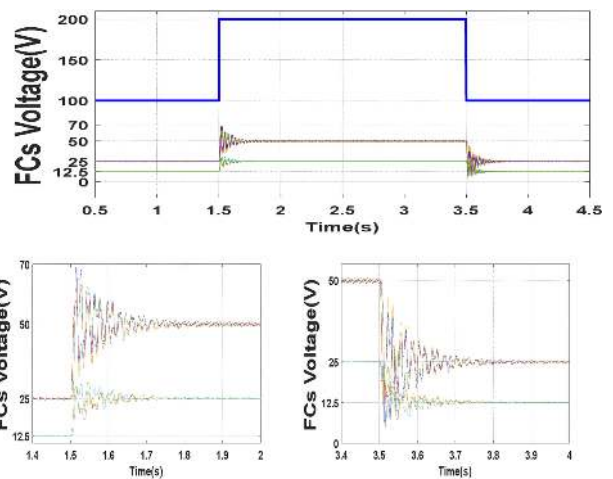

FIGURE 17. Dynamic response of ZPUC-MMC converter for a 100% step of DC voltage changing from 100 V to 200 V and then back to 100 V.
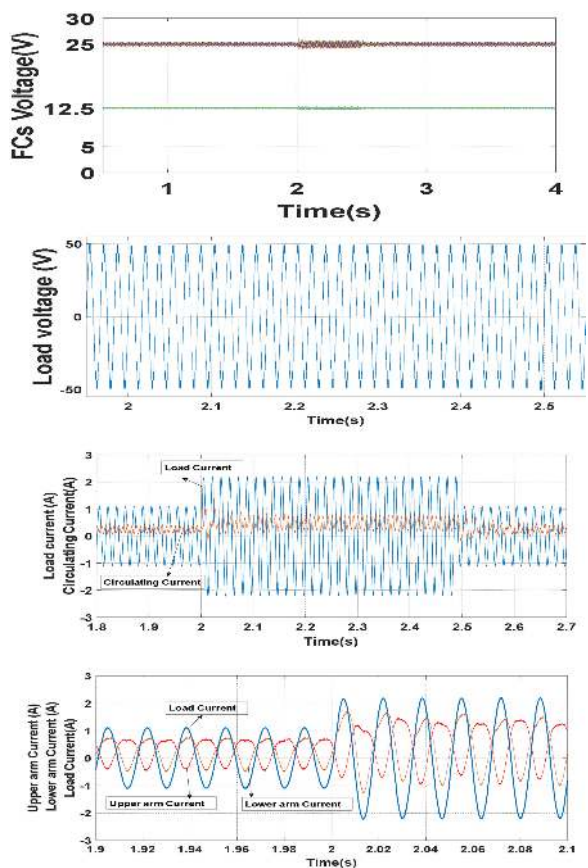

FIGURE 18. Wave forms of FCs voltage, load voltage, load current, upper arm current, upper arm current and circulating current during the load variation from 40 Ω–20 Ω–40 Ω.

The dynamic performance of ZPUC-MMC with two modules of ZPUC per arm during the DC source variation is illustrated in Fig. 16.

Voltages in all twelve FCs has been shown in Fig. 16. The voltages in FCs are balanced properly in steady state and in transient state with a sever DC voltage variation. As well, small value of voltage THD for 17-L phase voltage demonstrates that the output filter size can be very much reduced which reduces the cost of converter considerably.

To study the dynamic response of ZPUC-MMC converter a step of DC voltage changes representing the worst-case scenario on the DC link capacitor has been considered and the simulation results are depicted in Fig. 17. This figure shows the dynamic response of the converter when the DC source is varied by 100% from 100 V to 200 V and then back to 100 V. FCs voltages are completely stabilized within 200 ms, and the magnitude of voltage surge is less than 68 V. However, in practical application up to 20% of voltage variations can be tolerated in which the surge magnitude is consequently very limited.

Moreover, load current is another parameter which may be changed in stand-alone mode. Thus, in Fig. 18, performance of ZPUC-MMC with two modules per arm under the load variation is examined. The load is varied from 40 Ω to 20 Ω and again it comes back to its first value 40 Ω. The inductance was not changed in this test. FC voltages are balanced in their desired value which has been carried out by proposed

TABLE 8. Simulation Parameters of Grid-Connected Mode

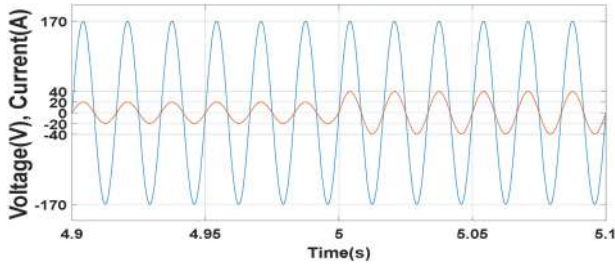|	
DC link voltage	400 VDC
Grid voltage	120 Vrms
Grid link inductor	2 mH
Capacitor C1, C2, C3	5000 µF
Reference current	20A
Refence power factor	1

FIGURE 19. Grid current and grid voltage during the variation in reference current from 20A to 40A and reference PF = 0.
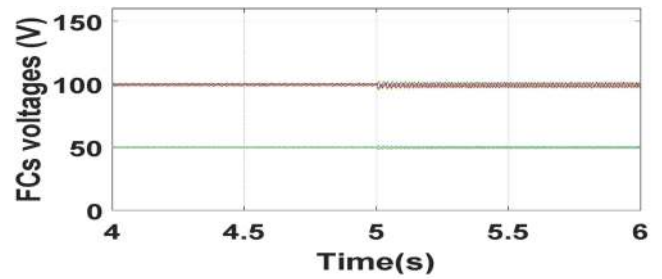

(a)

(b)

FIGURE 20. (a) FCs voltages and (b) upper arm voltage, lower arm voltage and inverter voltage during reference current changes from 20A to 40A and reference PF = 0.

voltage balancing method. However, the voltage ripple in FCs is increased due to the load current increase which is verifiable from the Eq. (30). As well, it is shown that the load voltage is constant during the load variation which verifies the performance of the converter. Moreover, circulating current and load current are shown in this figure which confirms the acceptable circulating current control through voltage balancing method integrated with the modulation technique.

However, additional control system can be used for complete elimination of circulating current which reduces the reliability and requires the more cost.

B. GRID-CONNECTED MODE

ZPUC-MMC with two modules per arm is considered for grid-connected operation so as to verify the performance of the proposed converter and the control.

As discussed in Section III. D, the PI control integrated with voltage balancing algorithm is used to current and power factor control. Dynamic response of ZPUC-MMC has been investigated in two transient mode including reference current variation and power factor variation. Simulation parameters are listed in Table 8 in which DC link voltage and FCs size has been altered due to current injection to the grid and voltage ripple control based on Eq. (30). Power factor and injected current are the parameters which must be controlled when the converter is connected to the grid. Thus, in transient state, these two parameters are severely varied to verify the performance of the converter. Fig. 19 illustrates the grid voltage and grid current at the same figure to show the power factor control and injected current control simultaneously. It can be seen that the grid current is changed from 20 A to 40 A based on reference current change and the phase shift between
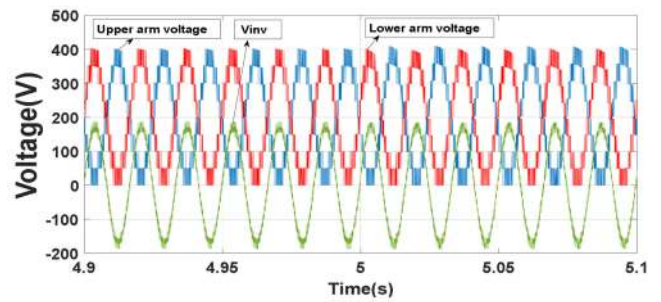
the grid current and grid voltage wave is zero which implies the performance of controller to make the reference PF = 0 exactly.

Fig. 20(a) depicts the FC voltages which shows the performance of voltage balancing algorithm and control system during the transient state due the load variation. Fig. 20(b) shows, upper and lower arm voltages which are placed in opposite phase shift based on the proposed voltage balancing control method. Nine level waveform is generated in each arm that make 17L waveform at the output of inverter due to using two ZPUC modules per arm.

Fig. 21 shows the circulating current and arms current that verifies the performance of voltage balancing integrated with modulation technique to mitigate it. THD of current which is injected into the grid through ZPUC converter shows extremely small value that are due to 17L voltage at the output of the inverter. This small value is useful to drastically reduce the filter size from the ZPUC inverter. Fig. 22 illustrates grid current and voltage as well as the voltage balancing in FCs during the power factor variation in which the PF was changed from 1 to 0 at t = 3 s and back to 1 at t = 3.2 s.

This fast-dynamic response also verifies the performance of ZPUC converter at transient state in grid connected mode.

V. EXPERIMENTAL RESULTS

Two 3 kVA module prototypes of ZPUC5 inverter have been built. They are assembled based on the configuration of Fig. 3 to validate the performance of topology and voltage balancing
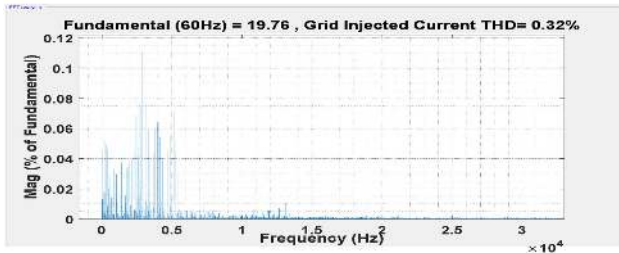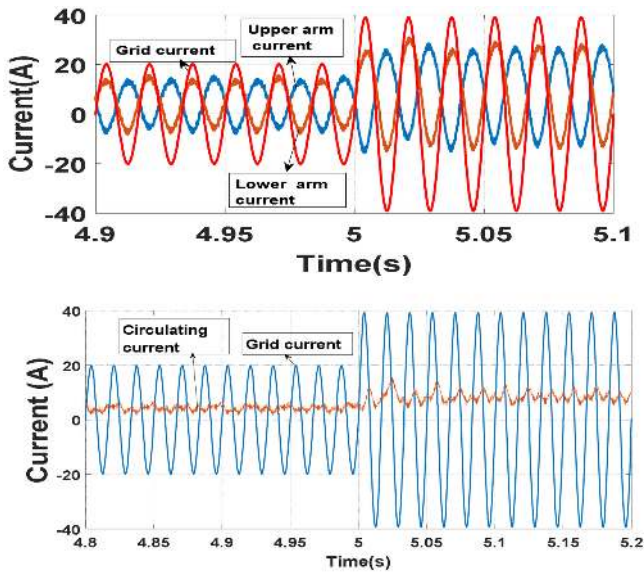
FIGURE 21. Current waveforms in upper arm, lower arm, load current, circulating current, and current THD during reference current variation from 20 A to 40 A and reference PF = 0.
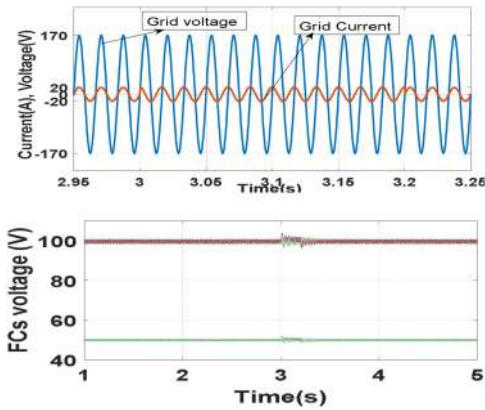

FIGURE 22. Grid connected waveforms, grid voltage and current during PF variations from 1 to 0 and again back to 1; and FCs voltage.

FIGURE 23. Experimental setup of the ZPUC multilevel converter.
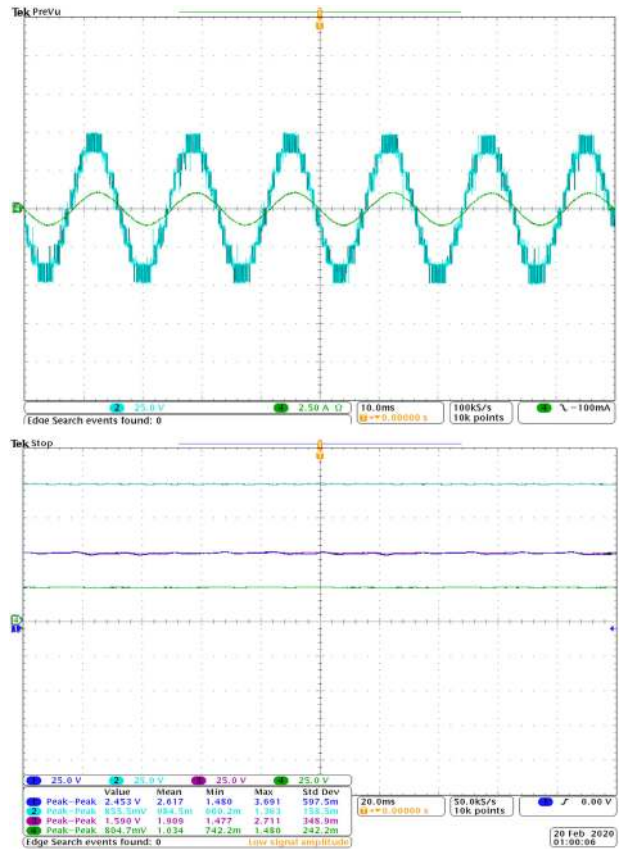
FIGURE 24. Load voltage, load current, and capacitor voltage balancing.

control method. The control algorithm of voltage balancing integrated with modulation technique has been implemented on dSpace 1103 as real-time controller and switching pulses are sent to the ZPUC5 switches in lower and upper arms through the dSpace 1103 interface board. ZPUC setup for experimental test in the lab is shown in Fig. 23. The parameters are the same as Table 7. Experimental results are
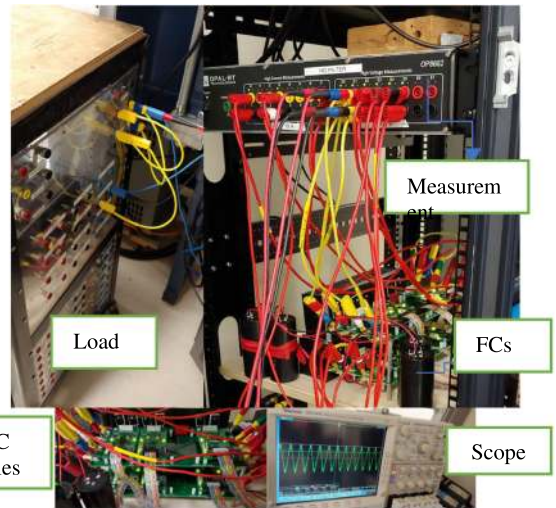
categorized based on steady state and transient mode to prove the performance of topology and controller. Fig. 24 shows the 9-L load voltage and current and capacitor voltages in the upper arm. DC source is 100v and two upper capacitors and one lower capacitor in each module of ZPUC are
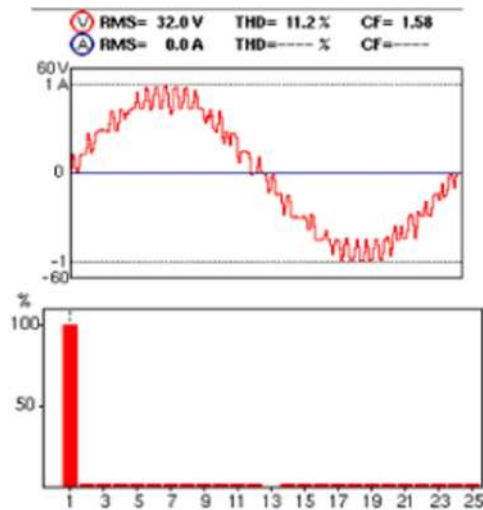
balanced in 50 V and 25 V respectively and the load voltage is established in steps of 25 V as illustrated in Fig. 24. The capacitor voltage ripple for two upper capacitors in each state is less than 2.5% and for lower capacitor is about 1% that shows the performance of the topology and the control method.

Fig. 25 shows the total harmonic distortion of ZPUC converter that is obtained through AEMC power analyzer which validates the lower THD due to its increased voltage levels.

As a transient study, load is varied from 40 ohm to 20 ohm and then it comes back to 40 ohm to examine the performance of the topology during the load variation in the inverter.

Fig. 26 shows that the load voltage is not varied due to the load variation which supports the performance of ZPUC converter in transient state. In addition, FCs voltages is depicted in this figure in which the DC value is constant that confirms the voltage balancing control method. Increase in the voltage ripple verifies the effect of the current load in voltage ripple based on Eq. (30).

Fig. 27 shows the variation in DC link voltage source which is increased from 100 V to 150 V and then back to 100 V. it can be seen from Fig. 27 that the flying capacitor voltages are balanced despite 50% changes in DC source which confirm the dynamic performance of the proposed voltage balancing control method.

Furthermore, Fig. 28 shows the load voltage and current waveforms through mentioned DC source variation. This figure shows the achievement of ZPUC converter and proposed control method to generate the voltage and current waveforms with a remarkable quality during the transient state as well as the steady state.

Finally, load voltage and current as well as capacitor voltages at C1 and C2 in upper arm in terms of changing the modulation index from 0.6 to 0.9 is shown in Fig. 29. ZPUC Converter generates 7-L waveform while modulation index is
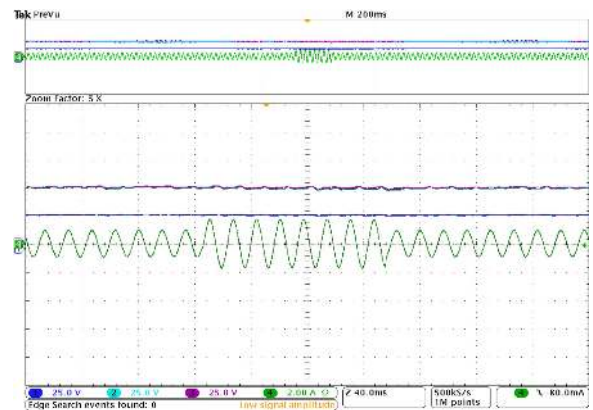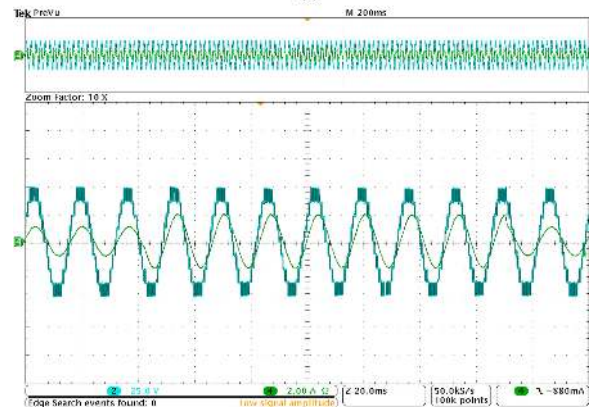
FIGURE 26. (a) FCs voltages and load current and (b) Load voltage and load current during the load variation from 40 Ω–20 Ω–40 Ω.
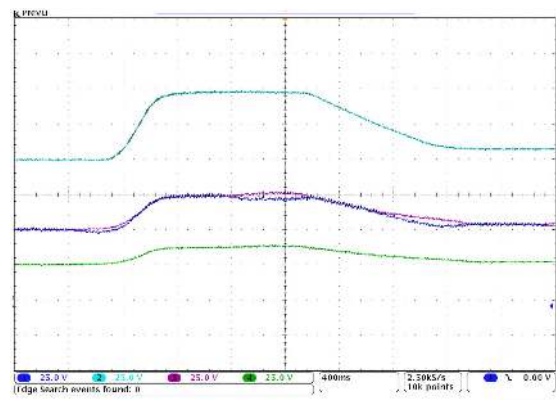

FIGURE 27. FCs voltage variation during the DC link voltage change. Channel 2 (light blue wave is the DC link voltage), Channel 1, and 3 are the voltage of C1 and C2 in upper arm module, Channel 4 is the voltage of C3 at upper arm module.

regulated in 0.6 and then it generates 9-L wave when modulation index is increased to 0.9. During these variations the voltage in the capacitors are still balanced and they are not changed that shows the performance and ability of converter to balance the voltages in FCs and consequently generating the high-quality output waveform.
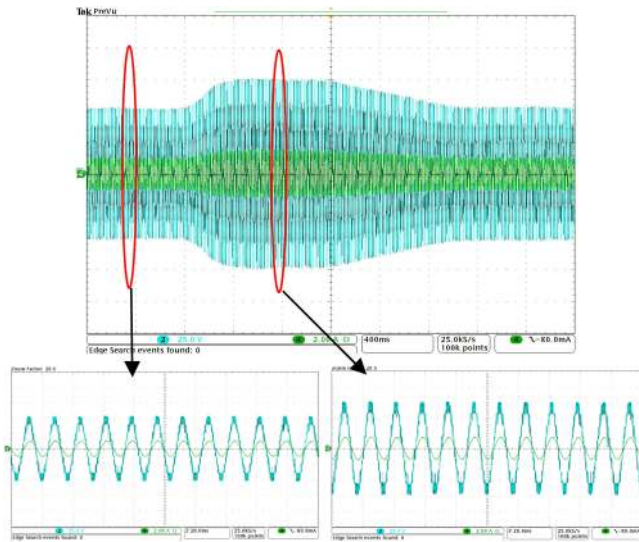
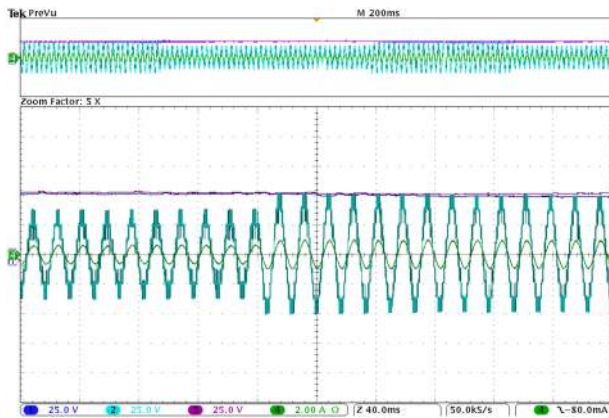**FIGURE 28.** Load voltage and current during the DC source variation.

FIGURE 29. Load voltage, load current, voltage in capacitors C1 and C2 during the modulation index variation from 0.6 to 0.9.

VI. CONCLUSION

ZPUC topology is a new multilevel converter that has been proposed in this paper. This topology can be utilized on rectifier or inverter modes as well as modular multilevel converters. Its application is motor drive, renewable energy integration to the grid, battery chargers, HVDC, STATCOM etc. As well, this topology could be a suitable alternative for multilevel converters in single-phase and three-phase system due to generating the high number of voltage levels, scalability and makes use of one DC source. This topology has some advantages compared to the other multilevel converters for single-phase and three-phase systems such as less component and switching devices, less power losses and more reliability. Voltage balancing in the capacitors are performed integrated with modulation strategy without any additional control loops. Appropriate voltage balancing algorithm for this topology has been presented in this paper. Simulation and experimental

results demonstrate that voltage regulation of three flying capacitors is tuned to their desired values and voltage across the load has been set to nine levels in steady states and transient modes.

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SAEED ARAZM (Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Mazandaran (Babol Noshirvani University of Technology), Babol, Iran, in 2004 and 2007 respectively. He is currently working toward the Ph.D. degree at the Ecole de Technologie Superieure, University of Quebec, Montreal, QC, Canada, as a Member of the Groupe de Recherche en Electronique de Puissance et Commande Industrielle. From 2006 to 2016, he was with Moshanir Power Engineering Consultant Company in High Voltage Department where he worked as a high voltage substation and power plant designer. He conducted power system studies in transient and steady state by Digsilent and EMTP-RV for many well-known projects. He was involved in the broad project of Tehran-Mashhad electrified railway with cooperation of Moshanir and Ineco Spain. From 2016 to 2017, he was with Iranian Powerplant Process Management (MAFNA) where he worked as a Lead Engineer for DG projects designs and related studies for grid connected. From 2017 to 2018, he was with GREPCI lab in ETS as a Research Engineer. His research interests include power electronics multilevel converters topology, control and modulation techniques, power quality, smart grid, high voltage, power system study, renewable energy conversion, electrified railway, and electric vehicles.

KAMAL AL-HADDAD (Fellow, IEEE) received the B.Sc.A. and M.Sc.A. degrees from the University of Québec à Trois-Rivières, Canada, in 1982 and 1984, respectively, and the Ph.D. degree from the Institute National Polytechnique, Toulouse, France, in 1988. Since June 1990, he has been a Professor with the Electrical Engineering Department, École de Technologie Supérieure (ETS), Montreal, QC, where he has been the holder of the senior Canada Research Chair in Electric Energy Conversion and Power Electronics since 2002. He has supervised more than 170 Ph.D. and M.Sc.A. students in the field of power electronics. He is a Consultant and has established very solid link with many Canadian industries working in the field of power electronics, energy conversion, electric transportation, renewable energy, multilevel topologies, aeronautics, and telecommunications. He has coauthored more than 600 transactions and conference papers as well as two books. Prof. Al-Haddad is a Fellow Member of the Canadian Academy of Engineering. He is IEEE IES President 2016-2017, Associate Editor of the Transactions on Industrial Informatics, IES Distinguished Lecturer and recipient of the 2014 IEEE IES Dr.-Ing. Eugene Mittelmann Achievement Award. Prof. Al-Haddad is a member of the Academy of Sciences and fellow of the Royal Society of Canada.