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ZrO_2 as a high-*k* dielectric for strained SiGe MOS devices

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Abstract. **The potential of ZrO_2 thin film as a high-*k* gate dielectric for scaled MOSFET devices has been studied. ZrO_2 has been deposited directly on a $Si_{0·8}Ge_{0·2}$ substrate by reactive RF magnetron sputtering. An equivalent oxide thickness of < 20 Å with a leakage current of the order of 10^{-4} A/cm^2 at 1 V has been obtained. Well-behaved capacitance–voltage characteristics with an interface state density of 2×10^{11} cm^{-2}eV^{-1} have been achieved. The deposited dielectric exhibits low charge trapping under constant current stressing.**

Keywords. **ZrO_2; high-*k* dielectric; SiGe MOS devices.**

1. Introduction

The enhancement of hole mobility in compressively strained SiGe layers deposited on Si is well known (People 1986; Crabbe *et al* 1992). However, the use of SiGe in mainstream metal–oxide–semiconductor field effect transistor (MOSFET) structures, has been plagued with the problems of poor gate oxides. In thermal oxidation of SiGe, the preferential oxidation of Si leads to the formation of Ge-rich layers at the oxide–substrate interface and causes serious degradation of oxide properties (LeGoues *et al* 1989). In addition, the strain relaxation of SiGe imposes serious thermal budget limitations (Hull *et al* 1988). These limitations have led to an interest for a new gate material deposited at low temperatures for SiGe devices. In recent years, high-*k* materials have drawn considerable attention as possible replacements for conventional Si oxide in ULSI. High-*k* materials such as Ta_2O_5 (Autran *et al* 1997; Luan *et al* 1998; Park *et al* 1998; van Dover *et al* 1998), TiO_2 (Guo *et al* 1998; He *et al* 1998) and strontium titanate (Mckee *et al* 1998) are not suitable for SiGe applications because they are not thermally stable on Si, and require a passivation barrier (oxynitride or nitride) to prevent interfacial layer growth. The passivation layers increase the process complexity and limit the scalability of the gate stack. ZrO_2 is one of few high-*k* materials that is predicted to be thermally stable on Si, based on a thermodynamic study (Hubbard and Scholm 1996). It has a high dielectric constant (20 ~ 25) and a large band gap (7·8 eV). The deposition and electrical properties of ZrO_2 on strained $Si_{1-x}Ge_x$ ($x = 20\%$) heterostructure have been investigated in this study and the results are presented.

2. Experimental

Lightly phosphorus doped Si wafers with a resistivity of 8–14 Ω-cm and ⟨001⟩ orientation were used as the starting substrate. *In situ* doped epitaxial layers of $Si_{0·8}Ge_{0·2}$ were deposited on Si buffer layer by ultra-high-vacuum chemical vapour deposition (UHVCVD) at 550°C using Si_2H_6, GeH_4 and PH_3. Prior to ZrO_2 deposition, the samples were subjected to a standard cleaning schedule followed by a dip for 1 min in dilute HF to remove the native oxide and to terminate the surface with hydrogen prior to loading in the process chamber. ZrO_2 was deposited by RF magnetron sputtering at a rf power 50 W with a base pressure 1×10^{-6} Torr. Reactive sputtering was performed in an Ar + O_2 ambient with the ratio 4 : 1 keeping the operating pressure of 1×10^{-1} Torr and the substrate temperature at 350°C.

Electrical characterizations of ZrO_2 films were carried out using fabricated Al–gate metal–insulator–semiconductor (MIS) capacitor structures. High frequency (100 kHz) capacitance–voltage (C–V) characteristics were used to extract the flat-band voltage (V_{FB}) and interface state density (D_{it}) at midgap energy. The d.c. current–voltage (I–V) characteristics were studied to evaluate the breakdown property of the MIS capacitors. Charge trapping behaviour of the dielectric was studied using constant current stressing of the capacitors.

3. Results and discussion

Semiconductor surface roughness is one of the important parameters, which can adversely affect the performance and reliability of the devices. Atomic force microscopy (AFM) was used to study the surface morphology of the film with a Nanoscope III system, from Digital Instruments. Figure 1 shows the atomic force micrograph of

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ZrO_2 film deposited on $Si_{0\cdot8}Ge_{0\cdot2}$. Root mean square roughness of deposited films is about 8·87 nm, which is higher than conventional thermal oxide grown on Si.

Figure 2 shows the high frequency (100 kHz) capacitance–voltage (*C–V*) characteristics of $Si/Si_{0\cdot8}Ge_{0\cdot2}/ZrO_2$/Al MIS structures. A well-behaved *C–V* curve is obtained with a relatively low value of flat band voltage. The capacitance in accumulation region is measured to be 8·24 nF, which corresponds to the equivalent silicon oxide thickness (EOT) = 1·83 nm. The dielectric constant of ZrO_2 films is found to be 20. The interface state density is calculated using Terman (1962) method. By comparison of the experimental 100 kHz *C–V* and the ideal high frequency *C–V* curve with the same equivalent oxide thickness, the interface state density is found to be $2\cdot0 \times 10^{11}$ cm^{-2} eV^{-1}. The magnitude is comparable to the best results published so far on the interfacial properties of gate oxides on SiGe layers (Tchikatilov *et al* 1996; Sharma *et al* 1999).

The key advantage offered by high-$\boldsymbol{k}$ materials is to increase the physical oxide thickness and reduce leakage currents without significantly increasing the actual EOT of gate dielectrics. The current density vs voltage (*J–V*) characteristics of ZrO_2 films is shown in figure 3. At a bias of 1 V, the leakage current density is around 10^{-4} A cm^{-2}. This is much lower than the leakage of SiO_2 gate oxide with the same equivalent oxide thickness (Buchanan and Lo 1997). The lower leakage current in ZrO_2 is attributed to the increased physical thickness of the higher dielectric constant material, and the high energy band gap of ZrO_2. Both the energy band gap of ZrO_2 (7·8 eV) and the increased physical thickness (due to high dielectric constant of ZrO_2) contribute to the reduction of tunnelling of carriers through the dielectric. It has been reported that the conduction band offset for ZrO_2 is 1·4 eV, while the valence band offset is 3·3 eV (Robertson *et al* 2000). These band offsets also indicate that the barrier heights for both electrons and holes are quite high leading to lower leakage current density in the film.

The charge trapping behaviour of ZrO_2 films under constant current stress of 10 mA/cm^2 for 300 s, measured by continuously monitoring the change in gate voltage (ΔV_G) required to maintain a constant current under gate injection, is presented in figure 4. The positive and negative gate voltage shifts indicate electron and hole trapping, respectively (Hao *et al* 1994). The gate voltage change, ΔV_G, is found to be – 100 mV for constant

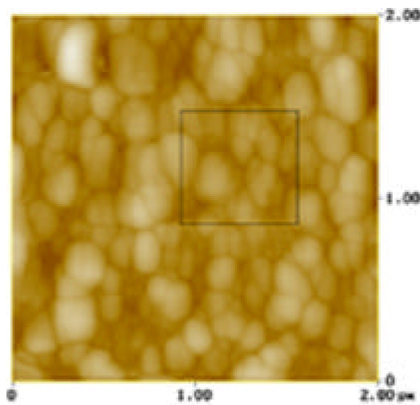

Figure 1. AFM micrograph of deposited ZrO_2 film on strained SiGe.

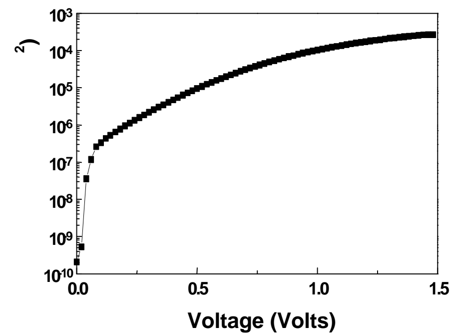

Figure 3. *J–V* characteristics of ZrO_2 films.

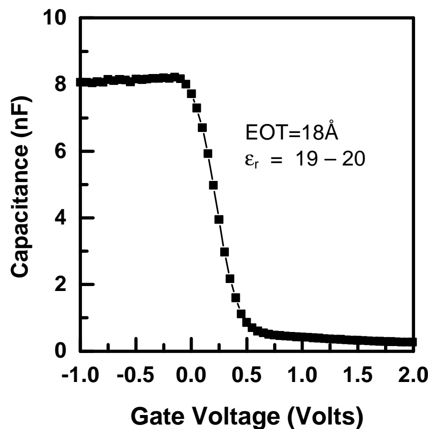

Figure 2. High frequency *C–V* characteristics of $Al/ZrO_2/Si_{0\cdot8}Ge_{0\cdot2}$/Si MIS structure.

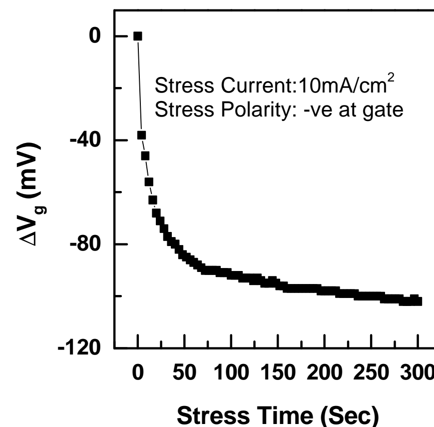

Figure 4. ΔV_G vs stress time of ZrO_2 on strained $Si_{0\cdot8}Ge_{0\cdot2}$ under a constant current stress.

current stress, indicating the hole trapping in the films. The presence of hole traps rather than electron traps in the oxide indicates the absence of any Ge segregation in the oxide–semiconductor interface during the oxidation process. The small ΔV_G also exhibits considerably lower charge trapping rates in deposited ZrO_2, making it highly attractive for SiGe MOS device applications.

4. Conclusions

We have demonstrated that ZrO_2 exhibits excellent electrical properties to become potential alternative to conventional SiO_2, especially for ULSI SiGe MOSFETs with gate oxide < 20 Å thick. ZrO_2 film with equivalent oxide thickness of < 20 Å has been achieved by RF sputtering. The interface state density of the dielectric on $Si_{0.8}Ge_{0.2}$ has been calculated to be 2×10^{11} cm^{-2} eV^{-1}. Experimental results show remarkably low leakage current, without any significant charge trapping under constant current stressing.

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